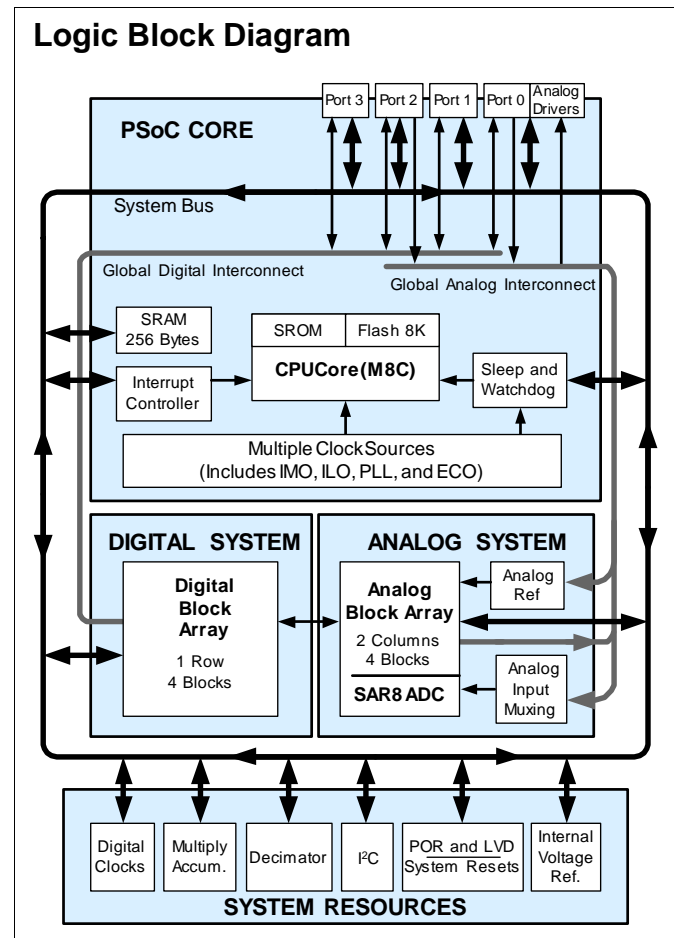


## Features

- **Powerful Harvard Architecture Processor**
  - M8C processor speeds to 24 MHz
  - 8x8 multiply, 32-bit accumulate
  - Low power at high speed
  - 3.0 to 5.25V operating voltage
  - Industrial temperature range: -40°C to +85°C
- **Advanced Peripherals (PSoC Blocks)**
  - 4 Rail-to-Rail analog PSoC Blocks provide:
    - Up to 14-bit ADCs
    - Up to 8-Bit DACs
    - Programmable gain amplifiers
    - Programmable filters and comparators
  - 4 Digital PSoC Blocks Provide:
    - 8- to 32-bit timers, counters, and PWMs
    - CRC and PRS modules
    - Full-duplex UART
    - Multiple SPI™ masters or slaves
    - Connectable to all GPIO pins
  - Complex peripherals by combining blocks
  - High-speed 8-bit SAR ADC optimized for motor control
- **Precision, Programmable Clocking**
  - Internal ±2.5% 24/48 MHz oscillator
  - High accuracy 24 MHz with optional 32 kHz crystal and PLL
  - Optional external oscillator, up to 24 MHz
  - Internal oscillator for watchdog and sleep
- **Flexible On-Chip Memory**
  - 8K Bytes Flash program storage 50,000 erase/write cycles
  - 256 Bytes SRAM data storage
  - In-System Serial Programming (ISSP)
  - Partial Flash updates
  - Flexible protection modes
  - EEPROM emulation in Flash
- **Programmable Pin Configurations**
  - 25 mA Sink on all GPIO
  - Pull up, pull down, High z, strong, or open drain drive modes on all GPIO
  - Up to 10 Analog inputs on GPIO
  - Two 30 mA Analog outputs on GPIO
  - Configurable interrupt on all GPIO
- **Additional System Resources**
  - I<sup>2</sup>C™ Slave, master, and multi-master to 400 kHz
  - Watchdog and sleep timers
  - User-configurable low voltage detection
  - Integrated supervisory circuit
  - On-chip precision voltage reference

- **Complete Development Tools**
  - Free development software (PSoC Designer™)
  - Full-featured in-circuit emulator and programmer
  - Full speed emulation
  - Complex breakpoint structure
  - 128K Bytes trace memory



## PSoC Functional Overview

The PSoC family consists of many Mixed-Signal Array with On-Chip Controller devices. These devices are designed to replace multiple traditional MCU-based system components with a low cost single-chip programmable device. PSoC devices include configurable blocks of analog and digital logic, and programmable interconnects. This architecture allows the user to create customized peripheral configurations that match the requirements of each individual application. Additionally, a fast CPU, Flash program memory, SRAM data memory, and configurable IO are included in a range of convenient pinouts and packages.

The PSoC architecture, as shown in the [Logic Block Diagram](#) on page 1, consists of four main areas: PSoC Core, Digital System, Analog System, and System Resources. Configurable global busing allows combining all the device resources into a complete custom system. The PSoC CY8C23x33 family can have up to three IO ports that connect to the global digital and analog interconnects, providing access to four digital blocks and four analog blocks.

### PSoC Core

The PSoC Core is a powerful engine that supports a rich feature set. The core includes a CPU, memory, clocks, and configurable GPIO (General Purpose IO).

The M8C CPU core is a powerful processor with speeds up to 24 MHz, providing a four MIPS 8-bit Harvard architecture microprocessor. The CPU uses an interrupt controller with 11 vectors, to simplify programming of real time embedded events. Program execution is timed and protected using the included Sleep and Watch Dog Timers (WDT).

Memory encompasses 8 KB of Flash for program storage, 256 bytes of SRAM for data storage, and up to 2 KB of EEPROM emulated using the Flash. Program Flash uses four protection levels on blocks of 64 bytes, allowing customized software IP protection.

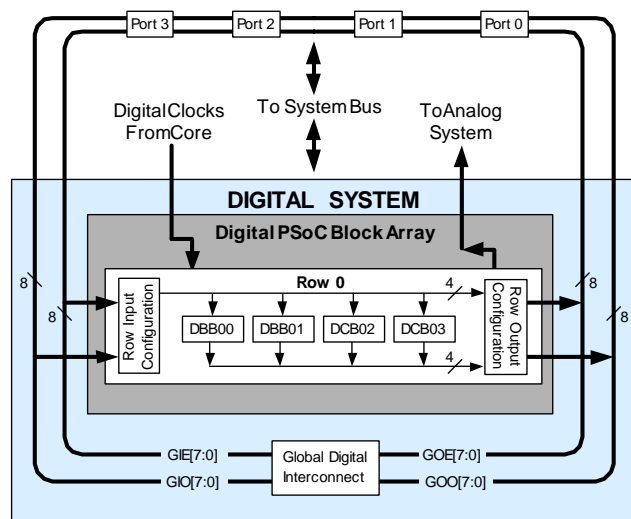
The PSoC device incorporates flexible internal clock generators, including a 24 MHz IMO (internal main oscillator) accurate to  $\pm 2.5\%$  over temperature and voltage. The 24 MHz IMO can also be doubled to 48 MHz for use by the digital system. A low power 32 kHz ILO (internal low speed oscillator) is provided for the Sleep timer and WDT. If crystal accuracy is desired, the ECO (32.768 kHz external crystal oscillator) is available for use as a Real Time Clock (RTC) and can optionally generate a crystal-accurate 24 MHz system clock using a PLL. The clocks, together with programmable clock dividers (as a System Resource), provide the flexibility to integrate almost any timing requirement into the PSoC device.

PSoC GPIOs provide connection to the CPU, digital and analog resources of the device. Each pin's drive mode may be selected from eight options, allowing great flexibility in external interfacing. Every pin also has the capability to generate a system interrupt on high level, low level, and change from last read.

## Digital System

The Digital System consists of 4 digital PSoC blocks. Each block is an 8-bit resource that is used alone or combined with other blocks to form 8, 16, 24, and 32-bit peripherals, which are called user module references.

Figure 1. Digital System Block Diagram



Digital peripheral configurations are:

- PWMs (8 to 32 bit)
- PWMs with Dead band (8 to 32 bit)
- Counters (8 to 32 bit)
- Timers (8 to 32 bit)
- UART 8 bit with selectable parity (up to 1)
- SPI master and slave (up to 1)
- I2C slave and master (1 available as a System Resource)
- Cyclical Redundancy Checker/Generator (8 to 32 bit)
- IrDA (up to 1)
- Pseudo Random Sequence Generators (8 to 32 bit)

The digital blocks can be connected to any GPIO through a series of global buses that can route any signal to any pin. The buses also allow for signal multiplexing and for performing logic operations. This configurability frees your designs from the constraints of a fixed peripheral controller.

Digital blocks are provided in rows of four, where the number of blocks varies by PSoC device family. This allows the optimum choice of system resources for your application. Family resources are shown in the table titled [PSoC Device Characteristics](#) on page 4.

## Analog System

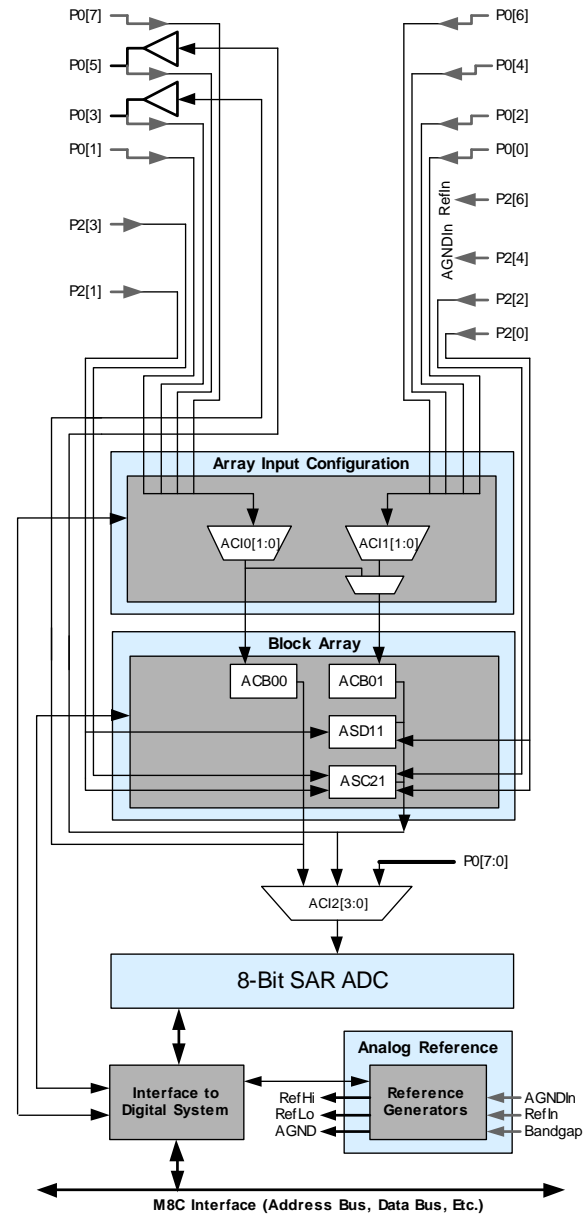
The Analog system consists of an 8-bit SAR ADC and four configurable blocks. The programmable 8-bit SAR ADC is an optimized ADC that runs up to 300 Ksps, with monotonic guarantee. It also has the features to support a motor control application.

Each analog block consists of an opamp circuit allowing the creation of complex analog signal flows. Analog peripherals are very flexible and can be customized to support specific application requirements. Some of the more common PSoC analog functions (most available as user modules) are:

- Filters (2 band pass, low-pass)
- Amplifiers (up to 2, with selectable gain to 48x)
- Instrumentation amplifiers (1 with selectable gain to 93x)
- Comparators (1, with 16 selectable thresholds)
- DAC (6 or 9-bit DAC)
- Multiplying DAC (6 or 9-bit DAC)
- High current output drivers (two with 30 mA drive)
- 1.3V reference (as a System Resource)
- DTMF dialer
- Modulators
- Correlators
- Peak detectors
- Many other topologies possible

Analog blocks are arranged in a column of three, which includes one CT (Continuous Time) and two SC (Switched Capacitor) blocks. The Analog Column 0 contains the SAR8 ADC block rather than the standard SC blocks.

Figure 2. Analog System Block Diagram



## Additional System Resources

System Resources, some of which are listed in the previous sections, provide additional capability useful to complete systems. Additional resources include a multiplier, decimator, low voltage detection, and power on reset. Brief statements describing the merits of each system resource follow:

- Digital clock dividers provide three customizable clock frequencies for use in applications. The clocks can be routed to both the digital and analog systems. Additional clocks can be generated using digital PSoC blocks as clock dividers.
- A multiply accumulate (MAC) provides a fast 8-bit multiplier with 32-bit accumulate, to assist in both general math and digital filters.
- The decimator provides a custom hardware filter for digital signal processing applications including the creation of Delta Sigma ADCs.
- The I2C module provides 100 and 400 kHz communication over two wires. Slave, master, and multi-master modes are all supported.
- Low Voltage Detection (LVD) interrupts can signal the application of falling voltage levels, while the advanced POR (Power On Reset) circuit eliminates the need for a system supervisor.
- An internal 1.3V reference provides an absolute reference for the analog system, including ADCs and DACs.

## PSoC Device Characteristics

Depending on the PSoC device characteristics, the digital and analog systems can have 16, 8, or 4 digital blocks and 12, 6, or 3 analog blocks. The following table lists the resources available for specific PSoC device groups.

**Table 1. PSoC Device Characteristics**

PSoC Part Number	Digital IO	Digital Rows	Digital Blocks	Analog Inputs	Analog Outputs	Analog Columns	Analog Blocks	SAR8 ADC
CY8C29x66	up to 64	4	16	12	4	4	12	No
CY8C27x43	up to 44	2	8	12	4	4	12	No
CY8C24x94	56	1	4	48	2	2	6	No
CY8C23X33	up to 26	1	4	12	2	2 <sup>[1]</sup>	4	Yes
CY8C24x23A	up to 24	1	4	12	2	2	6	No
CY8C21x34	up to 28	1	4	28	0	2	4 <sup>[2]</sup>	No
CY8C21x23	16	1	4	8	0	2	4 <sup>[2]</sup>	No
CY8C20x34	up to 28	0	0	28	0	0	3 <sup>[3]</sup>	No

### Notes

1. One complete column, plus one Continuous Time Block.
2. Limited analog functionality.
3. Two analog blocks and one CapSense

## Getting Started

The quickest path to understanding the PSoC silicon is by reading this data sheet and using the PSoC Designer Integrated Development Environment (IDE). This data sheet is an overview of the PSoC integrated circuit and presents specific pin, register, and electrical specifications. For in-depth information, along with detailed programming information, refer the *PSoC Mixed-Signal Array Technical Reference Manual*.

For latest Ordering, Packaging, and Electrical Specification information, refer the latest PSoC device data sheets on the web at <http://www.cypress.com/psoc>.

To determine which PSoC device meets your requirements, navigate through the PSoC Decision Tree in the Application Note AN2209 at <http://www.cypress.com> and select Application Notes under the Design Resources.

## Development Kits

Development Kits are available from the following distributors: Digi-Key, Avnet, Arrow, and Future. The Cypress Online Store contains development kits, C compilers, and all accessories for PSoC development. Go to the Cypress Online Store web site at <http://www.cypress.com/onlinestore>.

## Technical Training Modules

Free PSoC technical training modules are available for users new to PSoC. Training modules cover designing, debugging, advanced analog and CapSense. Go to <http://www.cypress.com>.

## Consultants

Certified PSoC Consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC Consultant go to <http://www.cypress.com>, click on Design Support located at the top of the web page, and select CYPros Consultants.

## Technical Support

PSoC application engineers take pride in fast and accurate response. They can be reached with a 4-hour guaranteed response at <http://www.cypress.com/support>.

## Application Notes

A long list of application notes can assist you in every aspect of your design effort. To view the PSoC application notes, go to <http://www.cypress.com/psocapnotes>.

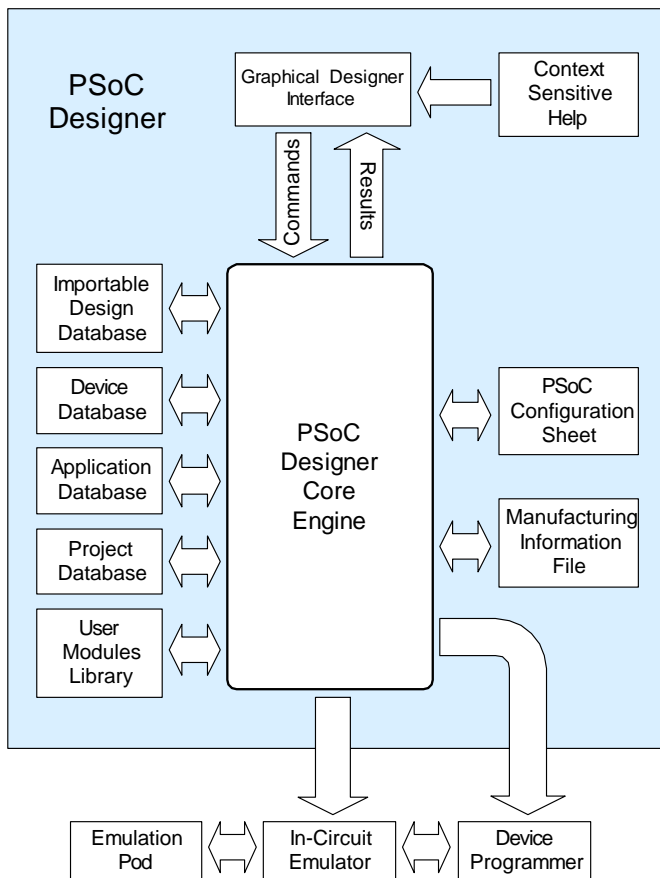
## Development Tools

PSoC Designer is a Microsoft® Windows-based, integrated development environment for the Programmable System-on-Chip (PSoC) devices. The PSoC Designer IDE and application runs on Windows NT 4.0, Windows 2000, Windows Millennium (Me), or Windows XP (refer [PSoC Designer Subsystems](#) on page 5).

PSoC Designer helps the customer to select an operating configuration for the PSoC, write application code that uses the PSoC, and debug the application. This system provides design database management by project, an integrated debugger with In-Circuit Emulator, in-system programming support, and the CYASM macro assembler for the CPUs.

PSoC Designer also supports a high-level C language compiler developed specifically for the devices in the family.

**Figure 3. PSoC Designer Subsystems**



## PSoC Designer Software Subsystems

### Device Editor

The Device Editor subsystem allows the user to select different onboard analog and digital components called user modules using the PSoC blocks. Examples of user modules are ADCs, DACs, Amplifiers, and Filters.

The device editor also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic configuration allows for changing configurations at run time.

PSoC Designer sets up power on initialization tables for selected PSoC block configurations and creates source code for an application framework. The framework contains software to operate the selected components and, if the project uses more than one operating configuration, contains routines to switch between different sets of PSoC block configurations at run time. PSoC Designer can print out a configuration sheet for a given project configuration for use during application programming in conjunction with the Device Data Sheet. Once the framework is generated, the user can add application-specific code to flesh out the framework. It is also possible to change the selected components and regenerate the framework.

### Design Browser

The Design Browser allows users to select and import preconfigured designs into the user's project. Users can easily browse a catalog of preconfigured designs to facilitate time-to-design. Examples provided in the tools include a 300-baud modem, LIN Bus master and slave, fan controller, and magnetic card reader.

### Application Editor

In the Application Editor you can edit your C language and Assembly language source code. You can also assemble, compile, link, and build.

**Assembler.** The macro assembler allows the assembly code to be merged seamlessly with C code. The link libraries automatically use absolute addressing or can be compiled in relative mode, and linked with other software modules to get absolute addressing.

**C Language Compiler.** A C language compiler is available that supports the PSoC family of devices. Even if you have never worked in the C language before, the product quickly allows you to create complete C programs for the PSoC family devices.

The embedded, optimizing C compiler provides all the features of C tailored to the PSoC architecture. It comes complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

*Debugger*

The PSoC Designer Debugger subsystem provides hardware in-circuit emulation, allowing the designer to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow the designer to read and program and read and write data memory, read and write IO registers, read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also allows the designer to create a trace buffer of registers and memory locations of interest.

*Online Help System*

The online help system displays online, context-sensitive help for the user. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an Online Support Forum to aid the designer in getting started.

**Hardware Tools**

*In-Circuit Emulator*

A low cost, high functionality ICE (In-Circuit Emulator) is available for development support. This hardware has the capability to program single devices.

The emulator consists of a base unit that connects to the PC by way of a USB port. The base unit is universal and can operate with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full speed (24 MHz) operation.

**Designing with User Modules**

The development process for the PSoC device differs from that of a traditional fixed function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and by lowering inventory costs. These configurable resources, called PSoC Blocks, have the ability to implement a wide variety of user-selectable functions. Each block has several registers that determine its function and connectivity to other blocks, multiplexers, buses and to the IO pins. Iterative development cycles permit you to adapt the hardware and the software. This substantially lowers the risk of having to select a different part to meet the final design requirements.

To speed the development process, the PSoC Designer Integrated Development Environment (IDE) provides a library of pre-built, pre-tested hardware peripheral functions, called "User Modules." User modules make selecting and implementing peripheral devices simple, and come in analog, digital, and mixed signal varieties. The standard User Module library contains over 50 common peripherals such as ADCs, DACs Timers, Counters, UARTs, and other uncommon peripherals such as DTMF Generators and Bi-Quad analog filter sections.

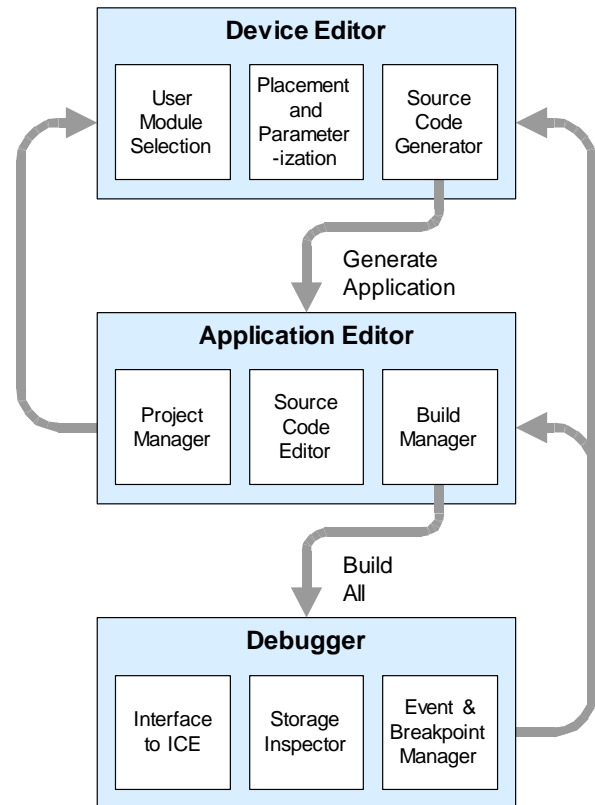
Each user module establishes the basic register settings that implement the selected function. It also provides parameters that allow you to tailor its precise configuration to your particular application. For example, a Pulse Width Modulator User Module configures one or more digital PSoC blocks, one for each 8 bits

of resolution. The user module parameters permit you to establish the pulse width and duty cycle. User modules also provide tested software to cut your development time. The user module application programming interface (API) provides high-level functions to control and respond to hardware events at run-time. The API also provides optional interrupt service routines that you can adapt as needed.

The API functions are documented in user module data sheets that are viewed directly in the PSoC Designer IDE. These data sheets explain the internal operation of the user module and provide performance specifications. Each data sheet describes the use of each user module parameter and documents the setting of each register controlled by the user module.

The development process starts when you open a new project and bring up the Device Editor, a graphical user interface (GUI) for configuring the hardware. You pick the user modules you need for your project and map them onto the PSoC blocks with point-and-click simplicity. Next, you build signal chains by interconnecting user modules to each other and the IO pins. At this stage, you also configure the clock source connections and enter parameter values directly or by selecting values from drop-down menus. When you are ready to test the hardware configuration or move on to developing code for the project, you perform the "Generate Application" step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the high-level user module API functions.

**Figure 4. User Module/Source Code Development Flows**



The next step is to write your main program, and any sub-routines using PSoC Designer's Application Editor subsystem. The Application Editor includes a Project Manager that allows you to open the project source code files (including all generated code files) from a hierarchal view. The source code editor provides syntax coloring and advanced edit features for both C and assembly language. File search capabilities include simple string searches and recursive "grep-style" patterns. A single mouse click invokes the Build Manager. It employs a professional-strength "makefile" system to automatically analyze all file dependencies and run the compiler and assembler as necessary. Project-level options control optimization strategies used by the compiler and linker. Syntax errors are displayed in a console window. Double clicking the error message takes you directly to the offending line of source code. When all is correct, the linker builds a HEX file image suitable for programming.

The last step in the development process takes place inside the PSoC Designer's Debugger subsystem. The Debugger downloads the HEX image to the In-Circuit Emulator (ICE) where it runs at full speed. Debugger capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint and watch-variable features, the Debugger provides a large trace buffer and allows you define complex breakpoint events that include monitoring address and data bus values, memory locations and external signals.

## Document Conventions

### Acronyms Used

The following table lists the acronyms that are used in this document.

Table 2. Acronyms Used

Acronym	Description
AC	alternating current
ADC	analog-to-digital converter
API	application programming interface
CPU	central processing unit
CT	continuous time
DAC	digital-to-analog converter
DC	direct current
EEPROM	electrically erasable programmable read-only memory
FSR	full scale range
GPIO	general purpose IO
IO	input/output
IPOR	imprecise power on reset
LSb	least-significant bit
LVD	low voltage detect
MSb	most-significant bit
PC	program counter
POR	power on reset
PPOR	precision power on reset
PSoC®	Programmable System-on-Chip™

Table 2. Acronyms Used (continued)

Acronym	Description
PWM	pulse width modulator
RAM	random access memory
ROM	read only memory
SC	switched capacitor

### Units of Measure

A units of measure table is located in the section [Electrical Specifications](#) on page 14. [Table 8](#) on page 14 lists all the abbreviations used to measure the PSoC devices.

### Numeric Naming

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase 'h' (for example, '14h' or '3Ah'). Hexadecimal numbers may also be represented by a '0x' prefix, the C coding convention. Binary numbers have an appended lowercase 'b' (for example, '01010100b' or '01000011b'). Numbers not indicated by an 'h' or 'b' are decimal.

## Pinouts

The PSoC CY8C23X33 is available in 32-pin QFN and 28-pin SSOP packages. Every port pin (labeled with a “P”), except for Vss and Vdd in the following table and illustration, is capable of Digital IO.

### 32-Pin Part Pinout

**Table 3. Pin Definitions - 32-Pin (QFN\*\*)**

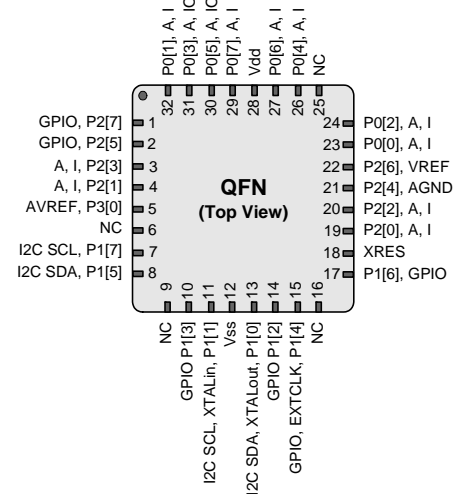
Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	IO		P2[7]	GPIO
2	IO		P2[5]	GPIO
3	IO	I	P2[3]	Direct Switched Capacitor Block Input
4	IO	I	P2[1]	Direct Switched Capacitor Block Input
5	IO	AVref	P3[0] <sup>4</sup>	GPIO/ADC Vref (optional)
6			NC	No Connection
7	IO		P1[7]	I2C Serial Clock (SCL)
8	IO		P1[5]	I2C Serial Data (SDA)
9			NC	No Connection
10	IO		P1[3]	GPIO
11	IO		P1[1]	GPIO, Crystal Input (XTALin), I2C Serial Clock (SCL), ISSP-SCLK*
12	Power		Vss	Ground Connection
13	IO		P1[0]	GPIO, Crystal Output (XTALout), I2C Serial Data (SDA), ISSP-SDATA*
14	IO		P1[2]	GPIO
15	IO		P1[4]	GPIO, External Clock IP
16			NC	No Connection
17	IO		P1[6]	GPIO
18	Input		XRES	Active High External Reset with Internal Pull Down
19	IO	I	P2[0]	Direct Switched Capacitor Block Input
20	IO	I	P2[2]	Direct Switched Capacitor Block Input
21	IO		P2[4]	External Analog Ground (AGnd)
22	IO		P2[6]	External Voltage Reference (VRef)
23	IO	I	P0[0]	Analog Column Mux Input and ADC Input
24	IO	I	P0[2]	Analog Column Mux Input and ADC Input
25			NC	No Connection
26	IO	I	P0[4]	Analog Column Mux Input and ADC Input
27	IO	I	P0[6]	Analog Column Mux Input and ADC Input
28	Power		Vdd	Supply Voltage
29	IO	I	P0[7]	Analog Column Mux Input and ADC Input
30	IO	IO	P0[5]	Analog Column Mux Input, Column Output and ADC Input
31	IO	IO	P0[3]	Analog Column Mux Input, Column Output and ADC Input
32	IO	I	P0[1]	Analog Column Mux Input and ADC Input

**LEGEND:** A = Analog, I = Input, and O = Output.

**Note**

- Even though P3[0] is an odd port, it resides on the left side of the pinout.

**Figure 5. CY8C23533 32-Pin PSoC Device**





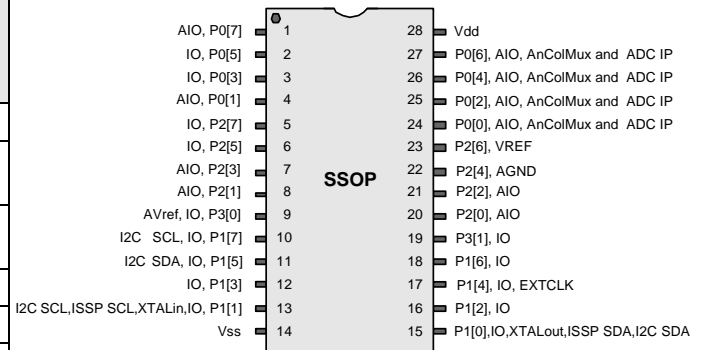
28-Pin Part Pinout

Table 4. Pin Definitions - 28-Pin (SSOP)

Pin Number CY8C23433	Digital	Analog	Pin Name	Description
1	IO	I	P0[7]	Analog Column Mux IP and ADC IP
2	IO	IO	P0[5]	Analog Column Mux IP and Column O/P and ADC IP
3	IO	IO	P0[3]	Analog Column Mux IP and Column O/P and ADC IP
4	IO	I	P0[1]	Analog Column Mux IP and ADC IP
5	IO		P2[7]	GPIO
6	IO		P2[5]	GPIO
7	IO	I	P2[3]	Direct Switched Capacitor Input
8	IO	I	P2[1]	Direct Switched Capacitor Input
9	IO	AVref	P3[0] <sup>[5]</sup>	GPIO/ADC Vref (optional)
10	IO		P1[7]	I2C SCL
11	IO		P1[5]	I2C SDA
12	IO		P1[3]	GPIO
13	IO		P1[1] <sup>[6]</sup>	GPIO, Xtal Input, I2C SCL, ISSP SCL
14	Power		Vss	Ground Pin
15	IO		P1[0] <sup>[6]</sup>	GPIO, Xtal Output, I2C SDA, ISSP SDA
16	IO		P1[2]	GPIO
17	IO		P1[4]	GPIO, External Clock IP
18	IO		P1[6]	GPIO
19	IO		P3[1] <sup>[7]</sup>	GPIO
20	IO	I	P2[0]	Direct Switched Capacitor Input
21	IO	I	P2[2]	Direct Switched Capacitor Input
22	IO		P2[4]	External Analog Ground (AGnd)
23	IO		P2[6]	Analog Voltage Reference (VRef)
24	IO	I	P0[0]	Analog Column Mux IP and ADC IP
25	IO	I	P0[2]	Analog Column Mux IP and ADC IP
26	IO	I	P0[4]	Analog Column Mux IP and ADC IP
27	IO	I	P0[6]	Analog Column Mux IP and ADC IP
28	Power		Vdd	Supply Voltage

LEGEND: A = Analog, I = Input, and O = Output.

Figure 6. CY8C23433 28-Pin PSoC Device



Notes

- 5. Even though P3[0] is an odd port, it resides on the left side of the pinout.
- 6. ISSP pin, which is not High Z at POR.
- 7. Even though P3[1] is an even port, it resides on the right side of the pinout.

## Register Reference

This section lists the registers of the CY8C23433 PSoC device by using mapping tables, in offset order.

### Register Conventions

#### *Abbreviations Used*

The register conventions specific to this section are listed in the following table.

**Table 5. Abbreviations**

Convention	Description
R	Read register or bits
W	Write register or bits
L	Logical register or bits
C	Clearable register or bits
#	Access is bit specific

## Register Mapping Tables

The PSoC device has a total register address space of 512 bytes. The register space is referred to as IO space and is divided into two banks. The XOI bit in the Flag register (CPU\_F) determines which bank the user is currently in. When the XOI bit is set the user is in Bank 1.

**Note** In the following register mapping tables, blank fields are reserved and must not be accessed.

Table 6. Register Map Bank 0 Table: User Space

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
PRT0DR	00	RW		40			80			C0	
PRT0IE	01	RW		41			81			C1	
PRT0GS	02	RW		42			82			C2	
PRT0DM2	03	RW		43			83			C3	
PRT1DR	04	RW		44		ASD11CR0	84	RW		C4	
PRT1IE	05	RW		45		ASD11CR1	85	RW		C5	
PRT1GS	06	RW		46		ASD11CR2	86	RW		C6	
PRT1DM2	07	RW		47		ASD11CR3	87	RW		C7	
PRT2DR	08	RW		48			88			C8	
PRT2IE	09	RW		49			89			C9	
PRT2GS	0A	RW		4A			8A			CA	
PRT2DM2	0B	RW		4B			8B			CB	
PRT3DR	0C	RW		4C			8C			CC	
PRT3IE	0D	RW		4D			8D			CD	
PRT3GS	0E	RW		4E			8E			CE	
PRT3DM2	0F	RW		4F			8F			CF	
	10			50			90			D0	
	11			51			91			D1	
	12			52			92			D2	
	13			53			93			D3	
	14			54		ASC21CR0	94	RW		D4	
	15			55		ASC21CR1	95	RW		D5	
	16			56		ASC21CR2	96	RW	I2C_CFG	D6	RW
	17			57		ASC21CR3	97	RW	I2C_SCR	D7	#
	18			58			98		I2C_DR	D8	RW
	19			59			99		I2C_MSCR	D9	#
	1A			5A			9A		INT_CLR0	DA	RW
	1B			5B			9B		INT_CLR1	DB	RW
	1C			5C			9C			DC	
	1D			5D			9D		INT_CLR3	DD	RW
	1E			5E			9E		INT_MSK3	DE	RW
	1F			5F			9F			DF	
DBB00DR0	20	#	AMX_IN	60	RW		A0		INT_MSK0	E0	RW
DBB00DR1	21	W		61			A1		INT_MSK1	E1	RW
DBB00DR2	22	RW		62			A2		INT_VC	E2	RC
DBB00CR0	23	#	ARF_CR	63	RW		A3		RES_WDT	E3	W
DBB01DR0	24	#	CMP_CR0	64	#		A4		DEC_DH	E4	RC
DBB01DR1	25	W	ASY_CR	65	#		A5		DEC_DL	E5	RC
DBB01DR2	26	RW	CMP_CR1	66	RW		A6		DEC_CR0	E6	RW
DBB01CR0	27	#	SARADC_DL	67	RW		A7		DEC_CR1	E7	RW
DCB02DR0	28	#		68			A8		MUL0_X	E8	W
DCB02DR1	29	W	SARADC_C0	69	#		A9		MUL0_Y	E9	W
DCB02DR2	2A	RW	SARADC_C1	6A	RW		AA		MUL0_DH	EA	R
DCB02CR0	2B	#		6B			AB		MUL0_DL	EB	R
DCB03DR0	2C	#	TMP_DR0	6C	RW		AC		ACC0_DR1	EC	RW
DCB03DR1	2D	W	TMP_DR1	6D	RW		AD		ACC0_DR0	ED	RW
DCB03DR2	2E	RW	TMP_DR2	6E	RW		AE		ACC0_DR3	EE	RW
DCB03CR0	2F	#	TMP_DR3	6F	RW		AF		ACC0_DR2	EF	RW
	30		ACB00CR3	70	RW	RDI0RI	B0	RW		F0	
	31		ACB00CR0	71	RW	RDI0SYN	B1	RW		F1	
	32		ACB00CR1	72	RW	RDI0IS	B2	RW		F2	
	33		ACB00CR2	73	RW	RDI0LT0	B3	RW		F3	
	34		ACB01CR3	74	RW	RDI0LT1	B4	RW		F4	
	35		ACB01CR0	75	RW	RDI0RO0	B5	RW		F5	
	36		ACB01CR1 *	76	RW	RDI0RO1	B6	RW		F6	
	37		ACB01CR2 *	77	RW		B7		CPU_F	F7	RL
	38			78			B8			F8	
	39			79			B9			F9	
	3A			7A			BA			FA	
	3B			7B			BB			FB	
	3C			7C			BC			FC	
	3D			7D			BD			FD	

Gray fields are reserved. # Access is bit specific.

**Table 6. Register Map Bank 0 Table: User Space (continued)**

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
	3E			7E			BE		CPU_SCR1	FE	#
	3F			7F			BF		CPU_SCR0	FF	#

Gray fields are reserved. # Access is bit specific.

**Table 7. Register Map Bank 1 Table: Configuration Space**

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
PRT0DM0	00	RW		40			80			C0	
PRT0DM1	01	RW		41			81			C1	
PRT0IC0	02	RW		42			82			C2	
PRT0IC1	03	RW		43			83			C3	
PRT1DM0	04	RW		44		ASD11CR0	84	RW		C4	
PRT1DM1	05	RW		45		ASD11CR1	85	RW		C5	
PRT1IC0	06	RW		46		ASD11CR2	86	RW		C6	
PRT1IC1	07	RW		47		ASD11CR3	87	RW		C7	
PRT2DM0	08	RW		48			88			C8	
PRT2DM1	09	RW		49			89			C9	
PRT2IC0	0A	RW		4A			8A			CA	
PRT2IC1	0B	RW		4B			8B			CB	
PRT3DM0	0C	RW		4C			8C			CC	
PRT3DM1	0D	RW		4D			8D			CD	
PRT3IC0	0E	RW		4E			8E			CE	
PRT3IC1	0F	RW		4F			8F			CF	
	10			50			90		GDI_O_IN	D0	RW
	11			51			91		GDI_E_IN	D1	RW
	12			52			92		GDI_O_OU	D2	RW
	13			53			93		GDI_E_OU	D3	RW
	14			54		ASC21CR0	94	RW		D4	
	15			55		ASC21CR1	95	RW		D5	
	16			56		ASC21CR2	96	RW		D6	
	17			57		ASC21CR3	97	RW		D7	
	18			58			98			D8	
	19			59			99			D9	
	1A			5A			9A			DA	
	1B			5B			9B			DB	
	1C			5C			9C			DC	
	1D			5D			9D		OSC_GO_EN	DD	RW
	1E			5E			9E		OSC_CR4	DE	RW
	1F			5F			9F		OSC_CR3	DF	RW
DBB00FN	20	RW	CLK_CR0	60	RW		A0		OSC_CR0	E0	RW
DBB00IN	21	RW	CLK_CR1	61	RW		A1		OSC_CR1	E1	RW
DBB00OU	22	RW	ABF_CR0	62	RW		A2		OSC_CR2	E2	RW
	23		AMD_CR0	63	RW		A3		VLT_CR	E3	RW
DBB01FN	24	RW		64			A4		VLT_CMP	E4	R
DBB01IN	25	RW		65			A5			E5	
DBB01OU	26	RW	AMD_CR1	66	RW		A6			E6	
	27		ALT_CR0	67	RW		A7			E7	
DCB02FN	28	RW		68		SARADC_TRS	A8	RW	IMO_TR	E8	W
DCB02IN	29	RW		69		SARADC_TRCL	A9	RW	ILO_TR	E9	W
DCB02OU	2A	RW		6A		SARADC_TRCH	AA	RW	BDG_TR	EA	RW
	2B			6B		SARADC_C2	AB	#	ECO_TR	EB	W
DCB03FN	2C	RW	TMP_DR0	6C	RW	SARADC_LCR	AC	RW		EC	
DCB03IN	2D	RW	TMP_DR1	6D	RW		AD			ED	
DCB03OU	2E	RW	TMP_DR2	6E	RW		AE			EE	
	2F		TMP_DR3	6F	RW		AF			EF	
	30		ACB00CR3	70	RW	RDI0RI	B0	RW		F0	
	31		ACB00CR0	71	RW	RDI0SYN	B1	RW		F1	
	32		ACB00CR1	72	RW	RDI0IS	B2	RW		F2	
	33		ACB00CR2	73	RW	RDI0LT0	B3	RW		F3	
	34		ACB01CR3	74	RW	RDI0LT1	B4	RW		F4	

Gray fields are reserved. # Access is bit specific.

**Table 7. Register Map Bank 1 Table: Configuration Space** (continued)

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
	35		ACB01CR0	75	RW	RDIO0R0	B5	RW		F5	
	36		ACB01CR1	76	RW	RDIO0R1	B6	RW		F6	
	37		ACB01CR2 *	77	RW		B7		CPU_F	F7	RL
	38			78			B8			F8	
	39			79			B9			F9	
	3A			7A			BA		FLS_PR1	FA	RW
	3B			7B			BB			FB	
	3C			7C			BC			FC	
	3D			7D			BD			FD	
	3E			7E			BE		CPU_SCR1	FE	#
	3F			7F			BF		CPU_SCR0	FF	#

Gray fields are reserved. # Access is bit specific.

## Electrical Specifications

This section presents the DC and AC electrical specifications of the CY8C23433 PSoC device. For the latest electrical specifications, visit <http://www.cypress.com/psoc>. Specifications are valid for  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$  and  $T_J \leq 100^{\circ}\text{C}$ , except where noted. Refer to Table 22 on page 25 for the electrical specifications on the internal main oscillator (IMO) using SLIMO mode.

Figure 7. Voltage versus CPU Frequency

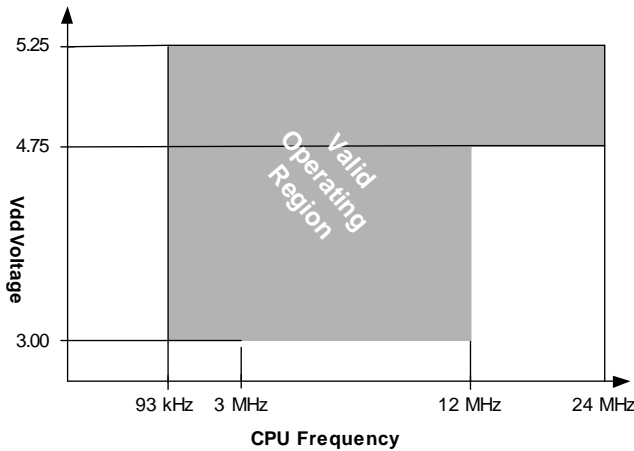
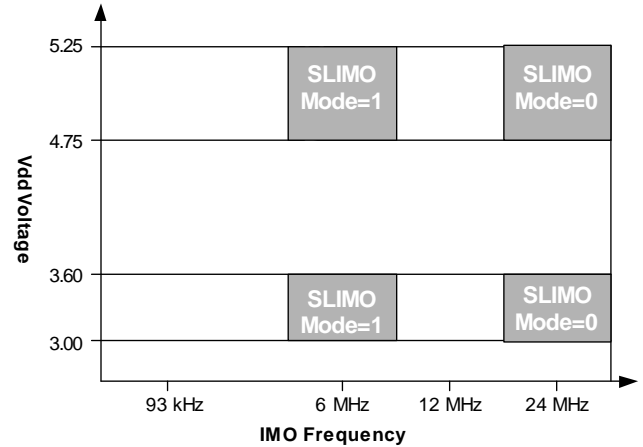


Figure 8. IMO Frequency Trim Options



The following table lists the units of measure that are used in this section.

Table 8. Units of Measure

Symbol	Unit of Measure	Symbol	Unit of Measure
$^{\circ}\text{C}$	degree Celsius	$\mu\text{W}$	micro watts
dB	decibels	mA	milli-ampere
fF	femto farad	ms	milli-second
Hz	hertz	mV	milli-volts
KB	1024 bytes	nA	nano ampere
Kbit	1024 bits	ns	nanosecond
kHz	kilohertz	nV	nanovolts
$k\Omega$	kilohm	W	ohm
MHz	megahertz	pA	pico ampere
$M\Omega$	megaohm	pF	pico farad
$\mu\text{A}$	micro ampere	pp	peak-to-peak
$\mu\text{F}$	micro farad	ppm	parts per million
$\mu\text{H}$	micro henry	ps	picosecond
$\mu\text{s}$	microsecond	sps	samples per second
$\mu\text{V}$	micro volts	s	sigma: one standard deviation
$\mu\text{Vrms}$	micro volts root-mean-square	V	volts

## Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Units	Notes
T <sub>STG</sub>	Storage Temperature	-55	25	+100	°C	Higher storage temperatures reduce data retention time. Recommended storage temperature is +25°C ± 25°C. Extended duration storage temperatures above 65°C degrade reliability.
T <sub>A</sub>	Ambient Temperature with Power Applied	-40	–	+85	°C	
V <sub>dd</sub>	Supply Voltage on V <sub>dd</sub> Relative to V <sub>ss</sub>	-0.5	–	+6.0	V	
V <sub>IO</sub>	DC Input Voltage	V <sub>ss</sub> - 0.5	–	V <sub>dd</sub> + 0.5	V	
V <sub>IOZ</sub>	DC Voltage Applied to Tri-state	V <sub>ss</sub> - 0.5	–	V <sub>dd</sub> + 0.5	V	
I <sub>MIO</sub>	Maximum Current into any Port Pin	-25	–	+50	mA	
ESD	Electro Static Discharge Voltage	2000	–	–	V	Human Body Model ESD.
LU	Latch-up Current	–	–	200	mA	

## Operating Temperature

Symbol	Description	Min	Typ	Max	Units	Notes
T <sub>A</sub>	Ambient Temperature	-40	–	+85	°C	
T <sub>J</sub>	Junction Temperature	-40	–	+100	°C	The temperature rise from ambient to junction is package specific. See <a href="#">Thermal Impedances by Package</a> on page 35. The user must limit the power consumption to comply with this requirement.

## DC Electrical Characteristics

### DC Chip-Level Specifications

The following table lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , or 3.0V to 3.6V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , respectively. Typical parameters apply to 5V and 3.3V at  $25^{\circ}\text{C}$  and are for design guidance only.

**Table 9. DC Chip-Level Specifications**

Symbol	Description	Min	Typ	Max	Units	Notes
V <sub>DD</sub>	Supply Voltage	3.0	–	5.25	V	See <a href="#">DC POR and LVD Specifications</a> on page 22.
I <sub>DD</sub>	Supply Current	–	5	8	mA	Conditions are V <sub>DD</sub> = 5.0V, T <sub>A</sub> = 25 °C, CPU = 3 MHz, SYSCLK doubler disabled, VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 93.75 kHz, analog power = off. SLIMO mode = 0. IMO = 24 MHz.
I <sub>DD3</sub>	Supply Current	–	3.3	6.0	mA	Conditions are V <sub>DD</sub> = 3.3V, T <sub>A</sub> = 25 °C, CPU = 3 MHz, SYSCLK doubler disabled, VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 93.75 kHz, analog power = off. SLIMO mode = 0. IMO = 24 MHz.
I <sub>SB</sub>	Sleep (Mode) Current with POR, LVD, Sleep Timer, and WDT. <sup>[8]</sup>	–	3	6.5	μA	Conditions are with internal slow speed oscillator, V <sub>DD</sub> = 3.3V, $-40^{\circ}\text{C} \leq T_A \leq 55^{\circ}\text{C}$ , analog power = off.
I <sub>SBH</sub>	Sleep (Mode) Current with POR, LVD, Sleep Timer, and WDT at high temperature. <sup>[8]</sup>	–	4	25	μA	Conditions are with internal slow speed oscillator, V <sub>DD</sub> = 3.3V, $55^{\circ}\text{C} < T_A \leq 85^{\circ}\text{C}$ , analog power = off.
I <sub>SBXTL</sub>	Sleep (Mode) Current with POR, LVD, Sleep Timer, WDT, and external crystal. <sup>[8]</sup>	–	4	7.5	μA	Conditions are with properly loaded, 1 μW max, 32.768 kHz crystal. V <sub>DD</sub> = 3.3V, $-40^{\circ}\text{C} \leq T_A \leq 55^{\circ}\text{C}$ , analog power = off.
I <sub>SBXTLH</sub>	Sleep (Mode) Current with POR, LVD, Sleep Timer, WDT, and external crystal at high temperature. <sup>[8]</sup>	–	5	26	μA	Conditions are with properly loaded, 1 μW max, 32.768 kHz crystal. V <sub>DD</sub> = 3.3 V, $55^{\circ}\text{C} < T_A \leq 85^{\circ}\text{C}$ , analog power = off.
V <sub>REF</sub>	Reference Voltage (Bandgap)	1.28	1.30	1.33	V	Trimmed for appropriate V <sub>DD</sub> . V <sub>DD</sub> > 3.0V.

**Note**

8. Standby current includes all functions (POR, LVD, WDT, Sleep Time) needed for reliable system operation. This must be compared with devices that have similar functions enabled.



**DC General Purpose IO Specifications**

The following table lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , or 3.0V to 3.6V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

**Table 10. 5V and 3.3V DC GPIO Specifications**

Symbol	Description	Min	Typ	Max	Units	Notes
R <sub>PU</sub>	Pull up Resistor	4	5.6	8	kΩ	
R <sub>PD</sub>	Pull down Resistor	4	5.6	8	kΩ	
V <sub>OH</sub>	High Output Level	V <sub>dd</sub> - 1.0	–	–	V	I <sub>OH</sub> = 10 mA, V <sub>dd</sub> = 4.75 to 5.25V (maximum 40 mA on even port pins (for example, P0[2], P1[4]), maximum 40 mA on odd port pins (for example, P0[3], P1[5])). 80 mA maximum combined IOH budget.
V <sub>OL</sub>	Low Output Level	–	–	0.75	V	I <sub>OL</sub> = 25 mA, V <sub>dd</sub> = 4.75 to 5.25V (maximum 100 mA on even port pins (for example, P0[2], P1[4]), maximum 100 mA on odd port pins (for example, P0[3], P1[5])). 100 mA maximum combined IOH budget.
V <sub>IL</sub>	Input Low Level	–	–	0.8	V	V <sub>dd</sub> = 3.0 to 5.25.
V <sub>IH</sub>	Input High Level	2.1	–	–	V	V <sub>dd</sub> = 3.0 to 5.25.
V <sub>H</sub>	Input Hysteresis	–	60	–	mV	
I <sub>IL</sub>	Input Leakage (Absolute Value)	–	1	–	nA	Gross tested to 1 μA.
C <sub>IN</sub>	Capacitive Load on Pins as Input	–	3.5	10	pF	Package and pin dependent. Temp = 25°C.
C <sub>OUT</sub>	Capacitive Load on Pins as Output	–	3.5	10	pF	Package and pin dependent. Temp = 25°C.

### DC Operational Amplifier Specifications

The following table lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , or 3.0V to 3.6V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

The Operational Amplifier is a component of both the Analog Continuous Time PSoC blocks and the Analog Switched Cap PSoC blocks. The guaranteed specifications are measured in the Analog Continuous Time PSoC block. Typical parameters apply to 5V at 25°C and are for design guidance only.

**Table 11. 5V DC Operational Amplifier Specifications**

Symbol	Description	Min	Typ	Max	Units	Notes
V <sub>OSOA</sub>	Input Offset Voltage (absolute value)	–	1.6	10	mV	
	Power = Low, Opamp Bias = High	–	1.3	8	mV	
	Power = Medium, Opamp Bias = High Power = High, Opamp Bias = High	–	1.2	7.5	mV	
TCV <sub>OSOA</sub>	Average Input Offset Voltage Drift	–	7.0	35.0	μV/°C	
I <sub>EBOA</sub>	Input Leakage Current (Port 0 Analog Pins)	–	20	–	pA	Gross tested to 1 μA.
C <sub>INOA</sub>	Input Capacitance (Port 0 Analog Pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25°C.
V <sub>CMOA</sub>	Common Mode Voltage Range	0.0	–	V <sub>dd</sub>	V	The common-mode input voltage range is measured through an analog output buffer. The specification includes the limitations imposed by the characteristics of the analog output buffer.
	Common Mode Voltage Range (high power or high opamp bias)	0.5	–	V <sub>dd</sub> - 0.5	V	
G <sub>OLOA</sub>	Open Loop Gain	–	–	–	dB	Specification is applicable at high power. For all other bias modes (except high power, high opamp bias), minimum is 60 dB.
	Power = Low, Opamp Bias = High	60	–	–	dB	
	Power = Medium, Opamp Bias = High Power = High, Opamp Bias = High	60 80	–	–	dB	
V <sub>OHIGHOA</sub>	High Output Voltage Swing (internal signals)	–	–	–	V	
	Power = Low, Opamp Bias = High	V <sub>dd</sub> - 0.2	–	–	V	
	Power = Medium, Opamp Bias = High Power = High, Opamp Bias = High	V <sub>dd</sub> - 0.2 V <sub>dd</sub> - 0.5	–	–	V	
V <sub>OLOWOA</sub>	Low Output Voltage Swing (internal signals)	–	–	0.2	V	
	Power = Low, Opamp Bias = High	–	–	0.2	V	
	Power = Medium, Opamp Bias = High Power = High, Opamp Bias = High	–	–	0.5	V	
I <sub>SOA</sub>	Supply Current (including associated AGND buffer)	–	300	400	μA	
	Power = Low, Opamp Bias = High	–	600	800	μA	
	Power = Medium, Opamp Bias = Low	–	1200	1600	μA	
	Power = Medium, Opamp Bias = High	–	2400	3200	μA	
	Power = High, Opamp Bias = Low	–	4600	6400	μA	
	Power = High, Opamp Bias = High	–	4600	6400	μA	
PSRR <sub>OA</sub>	Supply Voltage Rejection Ratio	52	80	–	dB	V <sub>ss</sub> ≤ VIN ≤ (V <sub>dd</sub> - 2.25) or (V <sub>dd</sub> - 1.25V) ≤ VIN ≤ V <sub>dd</sub> .

**Table 12. 3.3V DC Operational Amplifier Specifications**

Symbol	Description	Min	Typ	Max	Units	Notes
$V_{OSO A}$	Input Offset Voltage (absolute value) Power = Low, Opamp Bias = High Power = Medium, Opamp Bias = High High Power is 5 Volts Only	– –	1.65 1.32	10 8	mV mV	
$TCV_{OSO A}$	Average Input Offset Voltage Drift	–	7.0	35.0	$\mu V/^{\circ}C$	
$I_{EBO A}$	Input Leakage Current (Port 0 Analog Pins)	–	20	–	pA	Gross tested to 1 $\mu A$ .
$C_{INO A}$	Input Capacitance (Port 0 Analog Pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25 $^{\circ}C$ .
$V_{CMO A}$	Common Mode Voltage Range	0.2	–	Vdd - 0.2	V	The common-mode input voltage range is measured through an analog output buffer. The specification includes the limitations imposed by the characteristics of the analog output buffer.
$G_{OLO A}$	Open Loop Gain Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = Low Power = High, Opamp Bias = Low	60 60 80	–	–	dB	Specification is applicable at high power. For all other bias modes (except high power, high opamp bias), minimum is 60 dB.
$V_{OHIGHO A}$	High Output Voltage Swing (internal signals) Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = Low Power = High is 5V only	Vdd - 0.2 Vdd - 0.2 Vdd - 0.2	– – –	– – –	V V V	
$V_{OLOWO A}$	Low Output Voltage Swing (internal signals) Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = Low Power = High, Opamp Bias = Low	– – –	– – –	0.2 0.2 0.2	V V V	
$I_{SO A}$	Supply Current (including associated AGND buffer) Power = Low, Opamp Bias = High Power = Medium, Opamp Bias = Low Power = Medium, Opamp Bias = High Power = High, Opamp Bias = Low Power = High, Opamp Bias = High	– – – – –	300 600 1200 2400 4600	400 800 1600 3200 6400	$\mu A$ $\mu A$ $\mu A$ $\mu A$ $\mu A$	
$PSRR_{O A}$	Supply Voltage Rejection Ratio	52	80	–	dB	$V_{SS} \leq V_{IN} \leq (V_{DD} - 2.25)$ or $(V_{DD} - 1.25V) \leq V_{IN} \leq V_{DD}$ .

**DC Low Power Comparator Specifications**

The following table lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and  $-40^{\circ}C \leq T_A \leq 85^{\circ}C$ , or 3.0V to 3.6V and  $-40^{\circ}C \leq T_A \leq 85^{\circ}C$ , respectively. Typical parameters apply to 5V and 3.3V at 25 $^{\circ}C$  and are for design guidance only.

**Table 13. DC Low Power Comparator Specifications**

Symbol	Description	Min	Typ	Max	Units
$V_{REFLPC}$	Low power comparator (LPC) reference voltage range	0.2	–	Vdd - 1	V
$I_{SLPC}$	LPC supply current	–	10	40	$\mu A$
$V_{OSLPC}$	LPC voltage offset	–	2.5	30	mV

**DC Analog Output Buffer Specifications**

The following table lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , or 3.0V to 3.6V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

**Table 14. 5V DC Analog Output Buffer Specifications**

Symbol	Description	Min	Typ	Max	Units	Notes
$V_{OSOB}$	Input Offset Voltage (Absolute Value)	–	3	12	mV	
$TCV_{OSOB}$	Average Input Offset Voltage Drift	–	+6	–	$\mu\text{V}/^{\circ}\text{C}$	
$V_{CMOB}$	Common-Mode Input Voltage Range	0.5	–	Vdd - 1.0	V	
$R_{OUTOB}$	Output Resistance Power = Low Power = High	– –	1 1	– –	W W	
$V_{OHIGHOB}$	High Output Voltage Swing (Load = 32 ohms to Vdd/2) Power = Low Power = High	$0.5 \times V_{dd} + 1.1$ $0.5 \times V_{dd} + 1.1$	– –	– –	V V	
$V_{LOWOB}$	Low Output Voltage Swing (Load = 32 ohms to Vdd/2) Power = Low Power = High	– –	– –	$0.5 \times V_{dd} - 1.3$ $0.5 \times V_{dd} - 1.3$	V V	
$I_{SOB}$	Supply Current Including Bias Cell (No Load) Power = Low Power = High	– –	1.1 2.6	5.1 8.8	mA mA	
$PSRR_{OB}$	Supply Voltage Rejection Ratio	52	64	–	dB	$V_{OUT} > (V_{dd} - 1.25)$ .

**Table 15. 3.3V DC Analog Output Buffer Specifications**

Symbol	Description	Min	Typ	Max	Units	Notes
$V_{OSOB}$	Input Offset Voltage (Absolute Value)	–	3	12	mV	
$TCV_{OSOB}$	Average Input Offset Voltage Drift	–	+6	–	$\mu\text{V}/^{\circ}\text{C}$	
$V_{CMOB}$	Common-Mode Input Voltage Range	0.5	–	Vdd - 1.0	V	
$R_{OUTOB}$	Output Resistance Power = Low Power = High	– –	1 1	– –	W W	
$V_{OHIGHOB}$	High Output Voltage Swing (Load = 1k ohms to Vdd/2) Power = Low Power = High	$0.5 \times V_{dd} + 1.0$ $0.5 \times V_{dd} + 1.0$	– –	– –	V V	
$V_{LOWOB}$	Low Output Voltage Swing (Load = 1k ohms to Vdd/2) Power = Low Power = High	– –	– –	$0.5 \times V_{dd} - 1.0$ $0.5 \times V_{dd} - 1.0$	V V	
$I_{SOB}$	Supply Current Including Bias Cell (No Load) Power = Low Power = High	–	0.8 2.0	2.0 4.3	mA mA	
$PSRR_{OB}$	Supply Voltage Rejection Ratio	52	64	–	dB	$V_{OUT} > (V_{dd} - 1.25)$ .

**DC Analog Reference Specifications**

The following table lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , or 3.0V to 3.6V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

The guaranteed specifications are measured through the Analog Continuous Time PSoC blocks. The power levels for AGND refer to the power of the Analog Continuous Time PSoC block. The power levels for RefHi and RefLo refer to the Analog Reference Control register. The limits stated for AGND include the offset error of the AGND buffer local to the Analog Continuous Time PSoC block. Reference control power is high.

**Table 16. 5V DC Analog Reference Specifications**

Symbol	Description	Min	Typ	Max	Units
BG	Bandgap Voltage Reference	1.28	1.30	1.33	V
–	AGND = Vdd/2	Vdd/2 - 0.04	Vdd/2 - 0.01	Vdd/2 + 0.007	V
–	AGND = 2 x BandGap	2 x BG - 0.048	2 x BG - 0.030	2 x BG + 0.024	V
–	AGND = P2[4] (P2[4] = Vdd/2)	P2[4] - 0.011	P2[4]	P2[4] + 0.011	V
–	AGND = BandGap	BG - 0.009	BG + 0.008	BG + 0.016	V
–	AGND = 1.6 x BandGap	1.6 x BG - 0.022	1.6 x BG - 0.010	1.6 x BG + 0.018	V
–	AGND Block to Block Variation (AGND = Vdd/2)	-0.034	0.000	0.034	V
–	RefHi = Vdd/2 + BandGap	Vdd/2 + BG - 0.10	Vdd/2 + BG	Vdd/2 + BG + 0.10	V
–	RefHi = 3 x BandGap	3 x BG - 0.06	3 x BG	3 x BG + 0.06	V
–	RefHi = 2 x BandGap + P2[6] (P2[6] = 1.3V)	2 x BG + P2[6] - 0.113	2 x BG + P2[6] - 0.018	2 x BG + P2[6] + 0.077	V
–	RefHi = P2[4] + BandGap (P2[4] = Vdd/2)	P2[4] + BG - 0.130	P2[4] + BG - 0.016	P2[4] + BG + 0.098	V
–	RefHi = P2[4] + P2[6] (P2[4] = Vdd/2, P2[6] = 1.3V)	P2[4] + P2[6] - 0.133	P2[4] + P2[6] - 0.016	P2[4] + P2[6] + 0.100	V
–	RefHi = 3.2 x BandGap	3.2 x BG - 0.112	3.2 x BG	3.2 x BG + 0.076	V
–	RefLo = Vdd/2 – BandGap	Vdd/2 - BG - 0.04	Vdd/2 - BG + 0.024	Vdd/2 - BG + 0.04	V
–	RefLo = BandGap	BG - 0.06	BG	BG + 0.06	V
–	RefLo = 2 x BandGap - P2[6] (P2[6] = 1.3V)	2 x BG - P2[6] - 0.084	2 x BG - P2[6] + 0.025	2 x BG - P2[6] + 0.134	V
–	RefLo = P2[4] – BandGap (P2[4] = Vdd/2)	P2[4] - BG - 0.056	P2[4] - BG + 0.026	P2[4] - BG + 0.107	V
–	RefLo = P2[4]-P2[6] (P2[4] = Vdd/2, P2[6] = 1.3V)	P2[4] - P2[6] - 0.057	P2[4] - P2[6] + 0.026	P2[4] - P2[6] + 0.110	V

**Table 17. 3.3V DC Analog Reference Specifications**

Symbol	Description	Min	Typ	Max	Units
BG	Bandgap Voltage Reference	1.28	1.30	1.33	V
–	AGND = Vdd/2	Vdd/2 - 0.03	Vdd/2 - 0.01	Vdd/2 + 0.005	V
–	AGND = 2 x BandGap	Not Allowed			
–	AGND = P2[4] (P2[4] = Vdd/2)	P2[4] - 0.008	P2[4] + 0.001	P2[4] + 0.009	V
–	AGND = BandGap	BG - 0.009	BG + 0.005	BG + 0.015	V
–	AGND = 1.6 x BandGap	1.6 x BG - 0.027	1.6 x BG - 0.010	1.6 x BG + 0.018	V
–	AGND Column to Column Variation (AGND = Vdd/2)	-0.034	0.000	0.034	mV
–	RefHi = Vdd/2 + BandGap	Not Allowed			
–	RefHi = 3 x BandGap	Not Allowed			

**Table 17. 3.3V DC Analog Reference Specifications (continued)**

Symbol	Description	Min	Typ	Max	Units	
–	RefHi = 2 x BandGap + P2[6] (P2[6] = 0.5V)	Not Allowed				
–	RefHi = P2[4] + BandGap (P2[4] = Vdd/2)	Not Allowed				
–	RefHi = P2[4] + P2[6] (P2[4] = Vdd/2, P2[6] = 0.5V)	P2[4] + P2[6] - 0.075	P2[4] + P2[6] - 0.009	P2[4] + P2[6] + 0.057	V	
–	RefHi = 3.2 x BandGap	Not Allowed				
–	RefLo = Vdd/2 - BandGap	Not Allowed				
–	RefLo = BandGap	Not Allowed				
–	RefLo = 2 x BandGap - P2[6] (P2[6] = 0.5V)	Not Allowed				
–	RefLo = P2[4] - BandGap (P2[4] = Vdd/2)	Not Allowed				
–	RefLo = P2[4]-P2[6] (P2[4] = Vdd/2, P2[6] = 0.5V)	P2[4] - P2[6] - 0.048	P2[4]- P2[6] + 0.022	P2[4] - P2[6] + 0.092	V	

**DC Analog PSoC Block Specifications**

The following table lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , or 3.0V to 3.6V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

**Table 18. DC Analog PSoC Block Specifications**

Symbol	Description	Min	Typ	Max	Units
R <sub>CT</sub>	Resistor Unit Value (Continuous Time)	–	12.2	–	kΩ
C <sub>SC</sub>	Capacitor Unit Value (Switch Cap)	–	80 <sup>[9]</sup>	–	fF

**DC POR and LVD Specifications**

The following table lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , or 3.0V to 3.6V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

**Note** The bits PORLEV and VM in the following table refer to bits in the VLT\_CR register. See the *PSoC Mixed-Signal Array Technical Reference Manual* for more information on the VLT\_CR register.

**Table 19. DC POR and LVD Specifications**

Symbol	Description	Min	Typ	Max	Units	Notes
V <sub>PPOR1</sub> V <sub>PPOR2</sub>	Vdd Value for PPOR Trip PORLEV[1:0] = 01b PORLEV[1:0] = 10b	–	2.82 4.55	2.95 4.70	V V	Vdd must be greater than or equal to 2.5V during startup or reset from Watchdog.
V <sub>LVD1</sub> V <sub>LVD2</sub> V <sub>LVD3</sub> V <sub>LVD4</sub> V <sub>LVD5</sub> V <sub>LVD6</sub> V <sub>LVD7</sub>	Vdd Value for LVD Trip VM[2:0] = 001b VM[2:0] = 010b VM[2:0] = 011b VM[2:0] = 100b VM[2:0] = 101b VM[2:0] = 110b VM[2:0] = 111b	2.85 2.95 3.06 4.37 4.50 4.62 4.71	2.92 3.02 3.13 4.48 4.64 4.73 4.81	2.99 <sup>[10]</sup> 3.09 3.20 4.55 4.75 4.83 4.95	V V V V V V V	

**Notes**

9. C<sub>SC</sub> is a design guarantee parameter, not tested value

10. Always greater than 50 mV above V<sub>PPOR</sub> (PORLEV=01) for falling supply.

### DC Programming Specifications

The following table lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , or 3.0V to 3.6V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

**Table 20. DC Programming Specifications**

Symbol	Description	Min	Typ	Max	Units	Notes
V <sub>DDIWRITE</sub>	Supply Voltage for Flash Write Operations	2.7	–	–	V	
I <sub>DDP</sub>	Supply Current During Programming or Verify	–	5	25	mA	
V <sub>ILP</sub>	Input Low Voltage During Programming or Verify	–	–	0.8	V	
V <sub>IHP</sub>	Input High Voltage During Programming or Verify	2.1	–	–	V	
I <sub>ILP</sub>	Input Current when Applying V <sub>ilp</sub> to P1[0] or P1[1] During Programming or Verify	–	–	0.2	mA	Driving internal pull down resistor.
I <sub>IHP</sub>	Input Current when Applying V <sub>ihp</sub> to P1[0] or P1[1] During Programming or Verify	–	–	1.5	mA	Driving internal pull down resistor.
V <sub>OLV</sub>	Output Low Voltage During Programming or Verify	–	–	V <sub>SS</sub> + 0.75	V	
V <sub>OHV</sub>	Output High Voltage During Programming or Verify	V <sub>DD</sub> - 1.0	–	V <sub>DD</sub>	V	
Flash <sub>ENPB</sub>	Flash Endurance (per block)	50,000	–	–	–	Erase/write cycles per block.
Flash <sub>ENT</sub>	Flash Endurance (total) <sup>[11]</sup>	1,800,000	–	–	–	Erase/write cycles.
Flash <sub>DR</sub>	Flash Data Retention	10	–	–	Years	

**Note**

11. A maximum of 36 x 50,000 block endurance cycles is allowed. This may be balanced between operations on 36x1 blocks of 50,000 maximum cycles each, 36x2 blocks of 25,000 maximum cycles each, or 36x4 blocks of 12,500 maximum cycles each (to limit the total number of cycles to 36x50,000 and that no single block ever sees more than 50,000 cycles).

For the full industrial range, the user must employ a temperature sensor user module (FlashTemp) and feed the result to the temperature argument before writing. Refer to the Flash APIs Application Note AN2015 at <http://www.cypress.com> under Application Notes for more information.

**SAR8 ADC DC Specifications**

The following table lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , or 3.0V to 3.6V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

**Table 21. SAR8 ADC DC Specifications**

Symbol	Description	Min	Typ	Max	Units	Notes
$V_{\text{ADCVREF}}$	Reference voltage at pin P3[0] when configured as ADC reference voltage	3.0	–	5.25	V	The voltage level at P3[0] (when configured as ADC reference voltage) must always be maintained to be less than chip supply voltage level on Vdd pin. $V_{\text{ADCVREF}} < V_{\text{dd}}$ .
$I_{\text{ADCVREF}}$	Current when P3[0] is configured as ADC $V_{\text{REF}}$	3	–	–	mA	
INL	Integral Non-linearity	-1.5	–	+1.5	LSB	
INL (limited range)	Integral Non-linearity accommodating a shift in the offset at 0x80	-1.2 <sup>[12]</sup>	–	+1.2	LSB	The maximum LSB is over a sub-range not exceeding 1/16 of the full-scale range. 0x7F and 0x80 points specs are excluded here
DNL	Differential Non-linearity	-2.3	–	+2.3	LSB	ADC conversion is monotonic over full range
DNL (limited range)	Differential Non-linearity excluding 0x7F-0x80 transition	-1	–	+1	LSB	ADC conversion is monotonic over full range. 0x7F to 0x80 transition specs are excluded here.

**Notes**

12. SAR converters require a stable input voltage during the sampling period. If the voltage into the SAR8 changes by more than 1 LSB during the sampling period then the accuracy specifications may not be met



## AC Electrical Characteristics

### AC Chip-Level Specifications

The following table lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , or 3.0V to 3.6V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

**Table 22. 5V and 3.3V AC Chip-Level Specifications**

Symbol	Description	Min	Typ	Max	Units	Notes
F <sub>IMO24</sub>	Internal Main Oscillator Frequency for 24 MHz	23.4	24	24.6 <sup>[13],[14],[15]</sup>	MHz	Trimmed for 5V or 3.3V operation using factory trim values. See Figure 8 on page 14. SLIMO mode = 0.
F <sub>IMO6</sub>	Internal Main Oscillator Frequency for 6 MHz	5.75	6	6.35 <sup>[13],[14],[15]</sup>	MHz	Trimmed for 5V or 3.3V operation using factory trim values. See Figure 8 on page 14. SLIMO mode = 1.
F <sub>CPU1</sub>	CPU Frequency (5V Nominal)	0.093	24	24.6 <sup>[13],[14]</sup>	MHz	
F <sub>CPU2</sub>	CPU Frequency (3.3V Nominal)	0.093	12	12.3 <sup>[13],[14]</sup>	MHz	
F <sub>48M</sub>	Digital PSoC Block Frequency	0	48	49.2 <sup>[13],[14],[16]</sup>	MHz	Refer to the AC Digital Block Specifications.
F <sub>24M</sub>	Digital PSoC Block Frequency	0	24	24.6 <sup>[14],[16]</sup>	MHz	
F <sub>32K1</sub>	Internal Low Speed Oscillator Frequency	15	32	75	kHz	
F <sub>32K2</sub>	External Crystal Oscillator	–	32.768	–	kHz	Accuracy is capacitor and crystal dependent. 50% duty cycle.
F <sub>PLL</sub>	PLL Frequency	–	23.986	–	MHz	Is a multiple (x732) of crystal frequency.
Jitter24M2	24 MHz Period Jitter (PLL)	–	–	600	ps	
T <sub>PLLSLEW</sub>	PLL Lock Time	0.5	–	10	ms	
T <sub>PLLSLEWSLOW</sub>	PLL Lock Time for Low Gain Setting	0.5	–	50	ms	
T <sub>OS</sub>	External Crystal Oscillator Startup to 1%	–	1700	2620	ms	
T <sub>OSACC</sub>	External Crystal Oscillator Startup to 100 ppm	–	2800	3800	ms	The crystal oscillator frequency is within 100 ppm of its final value by the end of the T <sub>OSACC</sub> period. Correct operation assumes a properly loaded 1 uW maximum drive level 32.768 kHz crystal. 3.0V ≤ V <sub>DD</sub> ≤ 5.5V, -40°C ≤ T <sub>A</sub> ≤ 85°C.
Jitter32k	32 kHz Period Jitter	–	100	–	ns	
T <sub>XRST</sub>	External Reset Pulse Width	10	–	–	μs	
DC24M	24 MHz Duty Cycle	40	50	60	%	
Step24M	24 MHz Trim Step Size	–	50	–	kHz	
F <sub>out48M</sub>	48 MHz Output Frequency	46.8	48.0	49.2 <sup>[13],[15]</sup>	MHz	Trimmed. Using factory trim values.
Jitter24M1R	24 MHz Period Jitter (IMO) Root Mean Squared	–	–	600	ps	
F <sub>MAX</sub>	Maximum frequency of signal on row input or row output.	–	–	12.3	MHz	
T <sub>RAMP</sub>	Supply Ramp Time	0	–	–	μs	

#### Notes

13. 4.75V < V<sub>DD</sub> < 5.25V.

14. Accuracy derived from Internal Main Oscillator with appropriate trim for V<sub>DD</sub> range.

15. 3.0V < V<sub>DD</sub> < 3.6V. See Application Note AN2012 "Adjusting PSoC Microcontroller Trims for Dual Voltage-Range Operation" for information on trimming for operation at 3.3V.

16. See the individual user module data sheets for information on maximum frequencies for user modules.

Figure 9. PLL Lock Timing Diagram

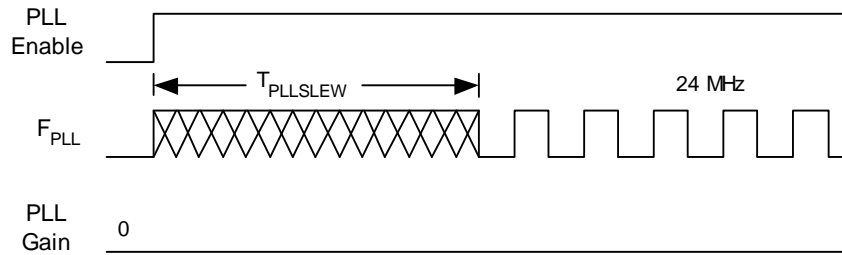


Figure 10. PLL Lock for Low Gain Setting Timing Diagram

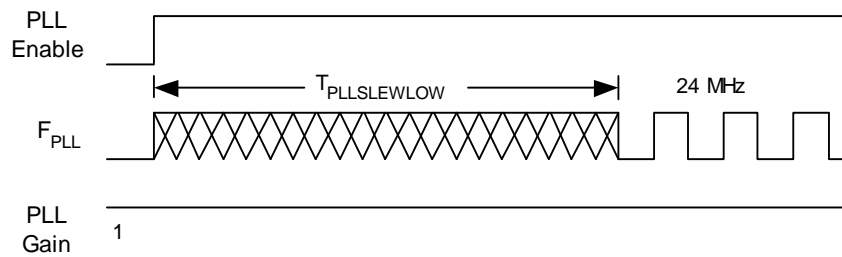


Figure 11. External Crystal Oscillator Startup Timing Diagram

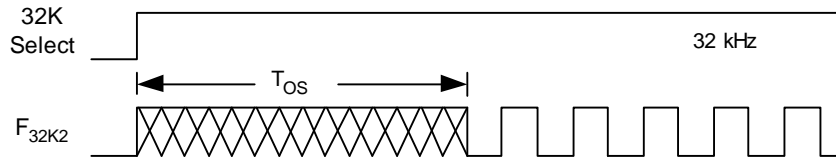


Figure 12. 24 MHz Period Jitter (IMO) Timing Diagram

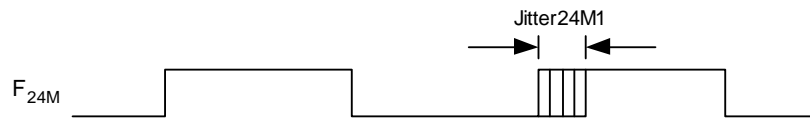
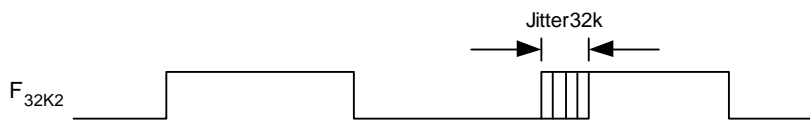


Figure 13. 32 kHz Period Jitter (ECO) Timing Diagram



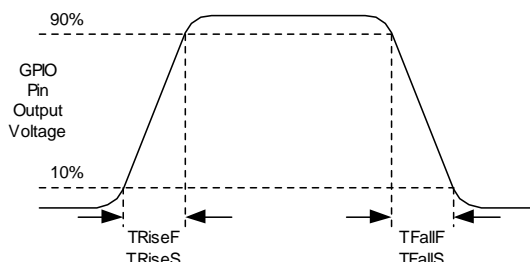
AC General Purpose IO Specifications

The following table lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , or 3.0V to 3.6V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 23. 5V and 3.3V AC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F <sub>GPIO</sub>	GPIO Operating Frequency	0	–	12.3	MHz	Normal Strong Mode
T <sub>RiseF</sub>	Rise Time, Normal Strong Mode, Clload = 50 pF	3	–	18	ns	V <sub>dd</sub> = 4.5 to 5.25V, 10% - 90%
T <sub>FallF</sub>	Fall Time, Normal Strong Mode, Clload = 50 pF	2	–	18	ns	V <sub>dd</sub> = 4.5 to 5.25V, 10% - 90%
T <sub>RiseS</sub>	Rise Time, Slow Strong Mode, Clload = 50 pF	10	27	–	ns	V <sub>dd</sub> = 3 to 5.25V, 10% - 90%
T <sub>FallS</sub>	Fall Time, Slow Strong Mode, Clload = 50 pF	10	22	–	ns	V <sub>dd</sub> = 3 to 5.25V, 10% - 90%

Figure 14. GPIO Timing Diagram



AC Operational Amplifier Specifications

The following table lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , or 3.0V to 3.6V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Settling times, slew rates, and gain bandwidth are based on the Analog Continuous Time PSoC block.

Power = High and Opamp Bias = High is not supported at 3.3V.

Table 24. 5V AC Operational Amplifier Specifications

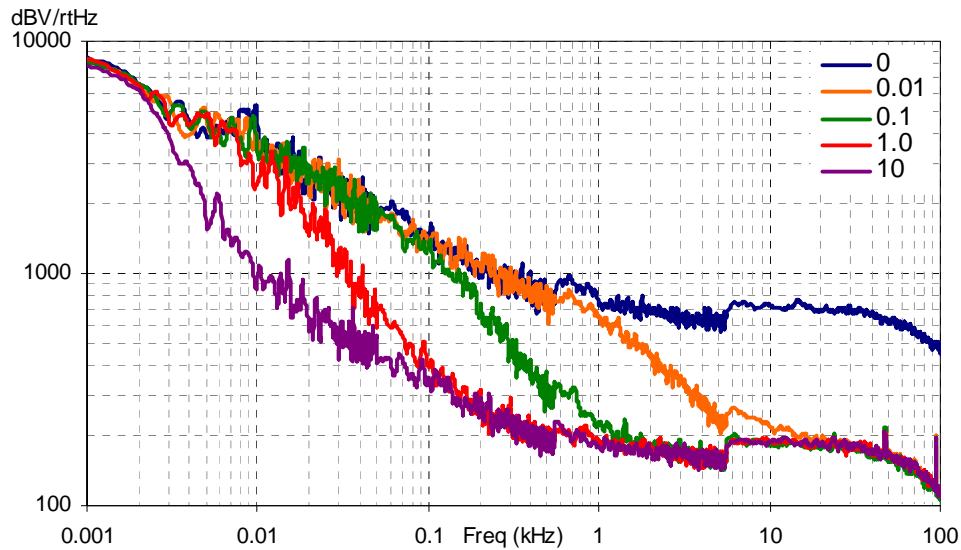
Symbol	Description	Min	Typ	Max	Units
T <sub>ROA</sub>	Rising Settling Time from 80% of ΔV to 0.1% of ΔV (10 pF load, Unity Gain)	–	–	3.9	μs
	Power = Low, Opamp Bias = Low	–	–	0.72	μs
	Power = High, Opamp Bias = High	–	–	0.62	μs
T <sub>SOA</sub>	Falling Settling Time from 20% of ΔV to 0.1% of ΔV (10 pF load, Unity Gain)	–	–	5.9	μs
	Power = Low, Opamp Bias = Low	–	–	0.92	μs
	Power = High, Opamp Bias = High	–	–	0.72	μs
SR <sub>ROA</sub>	Rising Slew Rate (20% to 80%)(10 pF load, Unity Gain)	0.15	–	–	V/μs
	Power = Low, Opamp Bias = Low	1.7	–	–	V/μs
	Power = High, Opamp Bias = High	6.5	–	–	V/μs
SR <sub>FOA</sub>	Falling Slew Rate (20% to 80%)(10 pF load, Unity Gain)	0.01	–	–	V/μs
	Power = Low, Opamp Bias = Low	0.5	–	–	V/μs
	Power = High, Opamp Bias = High	4.0	–	–	V/μs
BW <sub>OA</sub>	Gain Bandwidth Product	0.75	–	–	MHz
	Power = Low, Opamp Bias = Low	3.1	–	–	MHz
	Power = High, Opamp Bias = High	5.4	–	–	MHz

**Table 25. 3.3V AC Operational Amplifier Specifications**

Symbol	Description	Min	Typ	Max	Units
T <sub>ROA</sub>	Rising Settling Time from 80% of $\Delta V$ to 0.1% of $\Delta V$ (10 pF load, Unity Gain) Power = Low, Opamp Bias = Low	–	–	3.92	$\mu\text{s}$
	Power = Medium, Opamp Bias = High	–	–	0.72	$\mu\text{s}$
T <sub>SOA</sub>	Falling Settling Time from 20% of $\Delta V$ to 0.1% of $\Delta V$ (10 pF load, Unity Gain) Power = Low, Opamp Bias = Low	–	–	5.41	$\mu\text{s}$
	Power = Medium, Opamp Bias = High	–	–	0.72	$\mu\text{s}$
SR <sub>ROA</sub>	Rising Slew Rate (20% to 80%)(10 pF load, Unity Gain) Power = Low, Opamp Bias = Low	0.31	–	–	V/ $\mu\text{s}$
	Power = Medium, Opamp Bias = High	2.7	–	–	V/ $\mu\text{s}$
SR <sub>FOA</sub>	Falling Slew Rate (20% to 80%)(10 pF load, Unity Gain) Power = Low, Opamp Bias = Low	0.24	–	–	V/ $\mu\text{s}$
	Power = Medium, Opamp Bias = High	1.8	–	–	V/ $\mu\text{s}$
BW <sub>OA</sub>	Gain Bandwidth Product Power = Low, Opamp Bias = Low	0.67	–	–	MHz
	Power = Medium, Opamp Bias = High	2.8	–	–	MHz

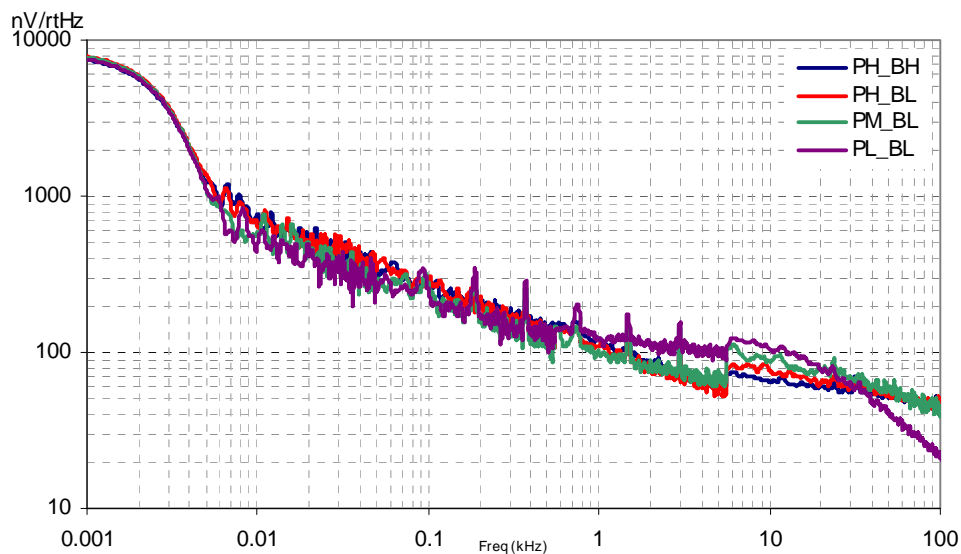
When bypassed by a capacitor on P2[4], the noise of the analog ground signal distributed to each block is reduced by a factor of up to 5 (14 dB). This is at frequencies above the corner frequency defined by the on-chip 8.1k resistance and the external capacitor.

Figure 15. Typical AGND Noise with P2[4] Bypass



At low frequencies, the opamp noise is proportional to  $1/f$ , power independent, and determined by device geometry. At high frequencies, increased power level reduces the noise spectrum level.

Figure 16. Typical Opamp Noise



**AC Low Power Comparator Specifications**

The following table lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , or 3.0V to 3.6V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

**Table 26. AC Low Power Comparator Specifications**

Symbol	Description	Min	Typ	Max	Units	Notes
T <sub>RLPC</sub>	LPC response time	–	–	50	μs	≥ 50 mV overdrive comparator reference set within V <sub>REFLPC</sub> .

**AC Digital Block Specifications**

The following table lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , or 3.0V to 3.6V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

**Table 27. 5V and 3.3V AC Digital Block Specifications**

Symbol	Description	Min	Typ	Max	Units	Notes
Timer	Capture Pulse Width	50 <sup>[17]</sup>	–	–	ns	
	Maximum Frequency, No Capture	–	–	49.2	MHz	4.75V < V <sub>dd</sub> < 5.25V.
	Maximum Frequency, With Capture	–	–	24.6	MHz	
Counter	Enable Pulse Width	50 <sup>[17]</sup>	–	–	ns	
	Maximum Frequency, No Enable Input	–	–	49.2	MHz	4.75V < V <sub>dd</sub> < 5.25V.
	Maximum Frequency, Enable Input	–	–	24.6	MHz	
Dead Band	Kill Pulse Width:					
	Asynchronous Restart Mode	20	–	–	ns	
	Synchronous Restart Mode	50 <sup>[17]</sup>	–	–	ns	
	Disable Mode	50 <sup>[17]</sup>	–	–	ns	
CRCPRS (PRS Mode)	Maximum Input Clock Frequency	–	–	49.2	MHz	4.75V < V <sub>dd</sub> < 5.25V.
	Maximum Input Clock Frequency	–	–	24.6	MHz	
SPIM	Maximum Input Clock Frequency	–	–	8.2	MHz	Maximum data rate at 4.1 MHz due to 2 x over clocking.
	Maximum Input Clock Frequency	–	–	4.1	MHz	
SPIS	Width of SS_ Negated Between Transmissions	50 <sup>[17]</sup>	–	–	ns	
	Maximum Input Clock Frequency	–	–	24.6	MHz	Maximum data rate at 3.08 MHz due to 8 x over clocking.
Transmitter	Maximum Input Clock Frequency with V <sub>dd</sub> ≥ 4.75V, 2 Stop Bits	–	–	49.2	MHz	Maximum data rate at 6.15 MHz due to 8 x over clocking.
	Maximum Input Clock Frequency	–	–	24.6	MHz	
Receiver	Maximum Input Clock Frequency	–	–	24.6	MHz	Maximum data rate at 3.08 MHz due to 8 x over clocking.
	Maximum Input Clock Frequency with V <sub>dd</sub> ≥ 4.75V, 2 Stop Bits	–	–	49.2	MHz	Maximum data rate at 6.15 MHz due to 8 x over clocking.

**Note**

17. 50 ns minimum input pulse width is based on the input synchronizers running at 24 MHz (42 ns nominal period).

**AC Analog Output Buffer Specifications**

The following table lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , or 3.0V to 3.6V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

**Table 28. 5V AC Analog Output Buffer Specifications**

Symbol	Description	Min	Typ	Max	Units
T <sub>ROB</sub>	Rising Settling Time to 0.1%, 1V Step, 100pF Load Power = Low Power = High	–	–	2.5	μs
		–	–	2.5	μs
T <sub>SOB</sub>	Falling Settling Time to 0.1%, 1V Step, 100pF Load Power = Low Power = High	–	–	2.2	μs
		–	–	2.2	μs
SR <sub>ROB</sub>	Rising Slew Rate (20% to 80%), 1V Step, 100pF Load Power = Low Power = High	0.65	–	–	V/μs
		0.65	–	–	V/μs
SR <sub>FOB</sub>	Falling Slew Rate (80% to 20%), 1V Step, 100pF Load Power = Low Power = High	0.65	–	–	V/μs
		0.65	–	–	V/μs
BW <sub>OB</sub>	Small Signal Bandwidth, 20mV <sub>pp</sub> , 3dB BW, 100pF Load Power = Low Power = High	0.8	–	–	MHz
		0.8	–	–	MHz
BW <sub>OB</sub>	Large Signal Bandwidth, 1V <sub>pp</sub> , 3dB BW, 100pF Load Power = Low Power = High	300	–	–	kHz
		300	–	–	kHz

**Table 29. 3.3V AC Analog Output Buffer Specifications**

Symbol	Description	Min	Typ	Max	Units
T <sub>ROB</sub>	Rising Settling Time to 0.1%, 1V Step, 100pF Load Power = Low Power = High	–	–	3.8	μs
		–	–	3.8	μs
T <sub>SOB</sub>	Falling Settling Time to 0.1%, 1V Step, 100pF Load Power = Low Power = High	–	–	2.6	μs
		–	–	2.6	μs
SR <sub>ROB</sub>	Rising Slew Rate (20% to 80%), 1V Step, 100pF Load Power = Low Power = High	0.5	–	–	V/μs
		0.5	–	–	V/μs
SR <sub>FOB</sub>	Falling Slew Rate (80% to 20%), 1V Step, 100pF Load Power = Low Power = High	0.5	–	–	V/μs
		0.5	–	–	V/μs
BW <sub>OB</sub>	Small Signal Bandwidth, 20mV <sub>pp</sub> , 3dB BW, 100pF Load Power = Low Power = High	0.7	–	–	MHz
		0.7	–	–	MHz
BW <sub>OB</sub>	Large Signal Bandwidth, 1V <sub>pp</sub> , 3dB BW, 100pF Load Power = Low Power = High	200	–	–	kHz
		200	–	–	kHz

### AC External Clock Specifications

The following table lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , or 3.0V to 3.6V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

**Table 30. 5V AC External Clock Specifications**

Symbol	Description	Min	Typ	Max	Units
F <sub>OSCEXT</sub>	Frequency	0.093	–	24.6	MHz
–	High Period	20.6	–	5300	ns
–	Low Period	20.6	–	–	ns
–	Power Up IMO to Switch	150	–	–	μs

**Table 31. 3.3V AC External Clock Specifications**

Symbol	Description	Min	Typ	Max	Units
F <sub>OSCEXT</sub>	Frequency with CPU Clock divide by 1 <sup>[18]</sup>	0.093	–	12.3	MHz
F <sub>OSCEXT</sub>	Frequency with CPU Clock divide by 2 or greater <sup>[19]</sup>	0.186	–	24.6	MHz
–	High Period with CPU Clock divide by 1	41.7	–	5300	ns
–	Low Period with CPU Clock divide by 1	41.7	–	–	ns
–	Power Up IMO to Switch	150	–	–	μs

### AC Programming Specifications

The following table lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , or 3.0V to 3.6V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

**Table 32. AC Programming Specifications**

Symbol	Description	Min	Typ	Max	Units	Notes
T <sub>RSCLK</sub>	Rise Time of SCLK	1	–	20	ns	
T <sub>FSCLK</sub>	Fall Time of SCLK	1	–	20	ns	
T <sub>SSCLK</sub>	Data Set up Time to Falling Edge of SCLK	40	–	–	ns	
T <sub>HSCLK</sub>	Data Hold Time from Falling Edge of SCLK	40	–	–	ns	
F <sub>SCLK</sub>	Frequency of SCLK	0	–	8	MHz	
T <sub>ERASEB</sub>	Flash Erase Time (Block)	–	20	–	ms	
T <sub>WRITE</sub>	Flash Block Write Time	–	20	–	ms	
T <sub>DSCLK</sub>	Data Out Delay from Falling Edge of SCLK	–	–	45	ns	V <sub>dd</sub> > 3.6
T <sub>DSCLK3</sub>	Data Out Delay from Falling Edge of SCLK	–	–	50	ns	3.0 ≤ V <sub>dd</sub> ≤ 3.6

### SAR8 ADC AC Specifications

The following table lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , or 3.0V to 3.6V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

**Table 33. SAR8 ADC AC Specifications<sup>[20]</sup>**

Symbol	Description	Min	Typ	Max	Units
Freq <sub>3</sub>	Input clock frequency 3V	–	–	3.075	MHz
Freq <sub>5</sub>	Input clock frequency 5V	–	–	3.075	MHz

**Notes**

18. Maximum CPU frequency is 12 MHz at 3.3V. With the CPU clock divider set to 1, the external clock must adhere to the maximum frequency and duty cycle requirements.

19. If the frequency of the external clock is greater than 12 MHz, the CPU clock divider must be set to 2 or greater. In this case, the CPU clock divider ensures that the fifty percent duty cycle requirement is met.

20. The max sample rate in this R2R ADC is 3.0/8=375KSPS



AC I<sup>2</sup>C Specifications

The following table lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , or 3.0V to 3.6V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

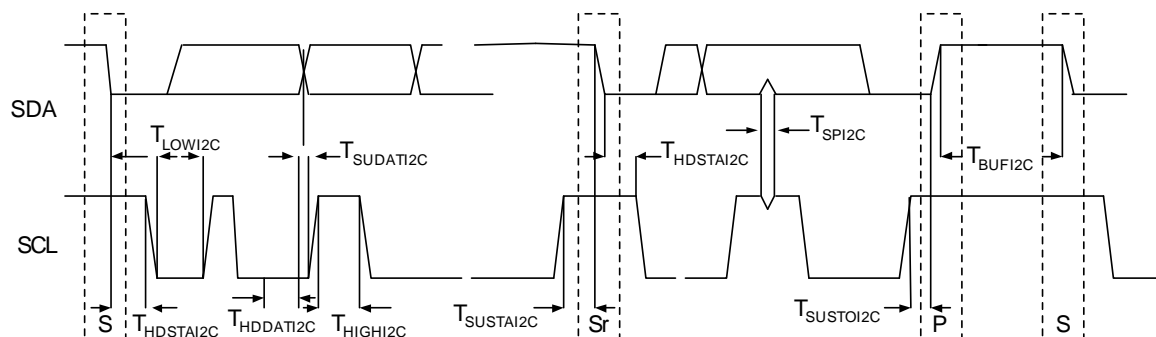
**Table 34. AC Characteristics of the I<sup>2</sup>C SDA and SCL Pins for Vdd > 3.0V**

Symbol	Description	Standard Mode		Fast Mode		Units
		Min	Max	Min	Max	
F <sub>SCL I2C</sub>	SCL Clock Frequency	0	100	0	400	kHz
T <sub>HDSTAI2C</sub>	Hold Time (repeated) START Condition. After this period, the first clock pulse is generated.	4.0	–	0.6	–	μs
T <sub>LOWI2C</sub>	LOW Period of the SCL Clock	4.7	–	1.3	–	μs
T <sub>HIGHI2C</sub>	HIGH Period of the SCL Clock	4.0	–	0.6	–	μs
T <sub>SUSTA I2C</sub>	Setup Time for a Repeated START Condition	4.7	–	0.6	–	μs
T <sub>HDDAT I2C</sub>	Data Hold Time	0	–	0	–	μs
T <sub>SUDAT I2C</sub>	Data Setup Time	250	–	100 <sup>[21]</sup>	–	ns
T <sub>SUSTOI2C</sub>	Setup Time for STOP Condition	4.0	–	0.6	–	μs
T <sub>BUFI2C</sub>	Bus Free Time Between a STOP and START Condition	4.7	–	1.3	–	μs
T <sub>SPI2C</sub>	Pulse Width of spikes are suppressed by the input filter.	–	–	0	50	ns

**Table 35. AC Characteristics of the I<sup>2</sup>C SDA and SCL Pins for Vdd < 3.0V (Fast Mode Not Supported)**

Symbol	Description	Standard Mode		Fast Mode		Units
		Min	Max	Min	Max	
F <sub>SCL I2C</sub>	SCL Clock Frequency	0	100	–	–	kHz
T <sub>HDSTAI2C</sub>	Hold Time (repeated) START Condition. After this period, the first clock pulse is generated.	4.0	–	–	–	μs
T <sub>LOWI2C</sub>	LOW Period of the SCL Clock	4.7	–	–	–	μs
T <sub>HIGHI2C</sub>	HIGH Period of the SCL Clock	4.0	–	–	–	μs
T <sub>SUSTA I2C</sub>	Setup Time for a Repeated START Condition	4.7	–	–	–	μs
T <sub>HDDAT I2C</sub>	Data Hold Time	0	–	–	–	μs
T <sub>SUDAT I2C</sub>	Data Setup Time	250	–	–	–	ns
T <sub>SUSTOI2C</sub>	Setup Time for STOP Condition	4.0	–	–	–	μs
T <sub>BUFI2C</sub>	Bus Free Time Between a STOP and START Condition	4.7	–	–	–	μs
T <sub>SPI2C</sub>	Pulse Width of spikes are suppressed by the input filter.	–	–	–	–	ns

**Figure 17. Definition for Timing for Fast/Standard Mode on the I<sup>2</sup>C Bus**



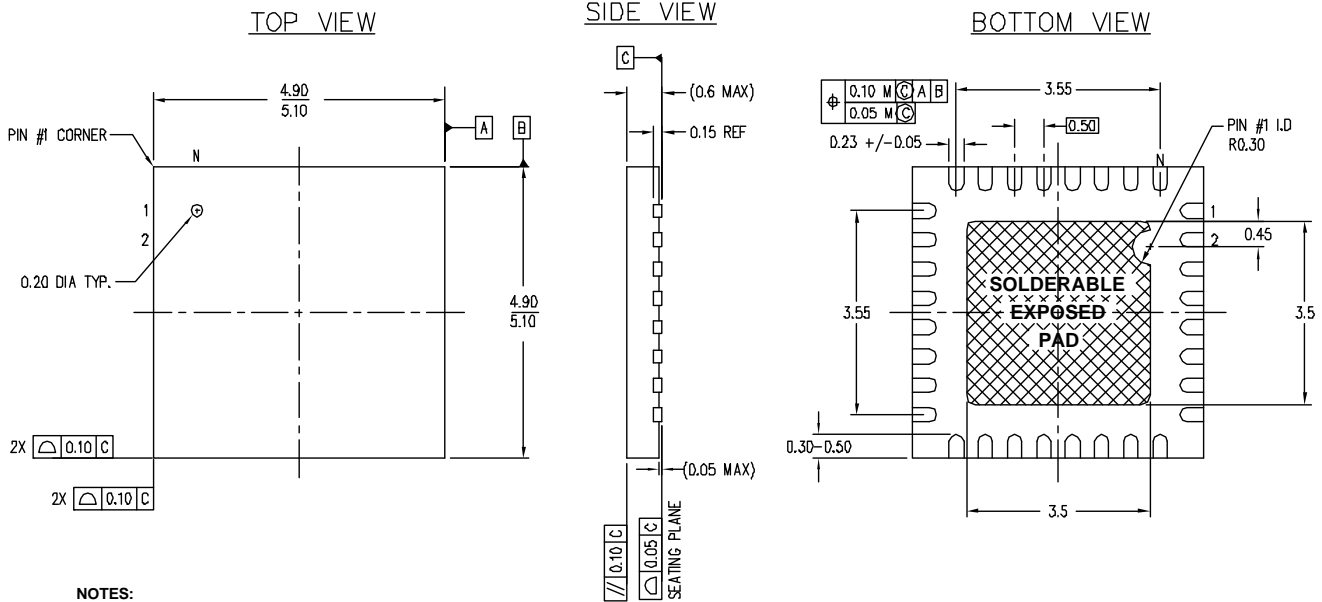
**Note**

21. A Fast-Mode I<sup>2</sup>C-bus device can be used in a Standard-Mode I<sup>2</sup>C-bus system, but the requirement  $t_{SU, DAT} \geq 250$  ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line  $t_{rmax} + t_{SU, DAT} = 1000 + 250 = 1250$  ns (according to the Standard-Mode I<sup>2</sup>C-bus specification) before the SCL line is released.


### Packaging Information

This section illustrates the packaging specifications for the CY8C23X33 PSoC device, along with the thermal impedances for each package, solder reflow peak temperature, and the typical package capacitance on crystal pins.

Figure 19. 32-Pin (5x5 mm) QFN



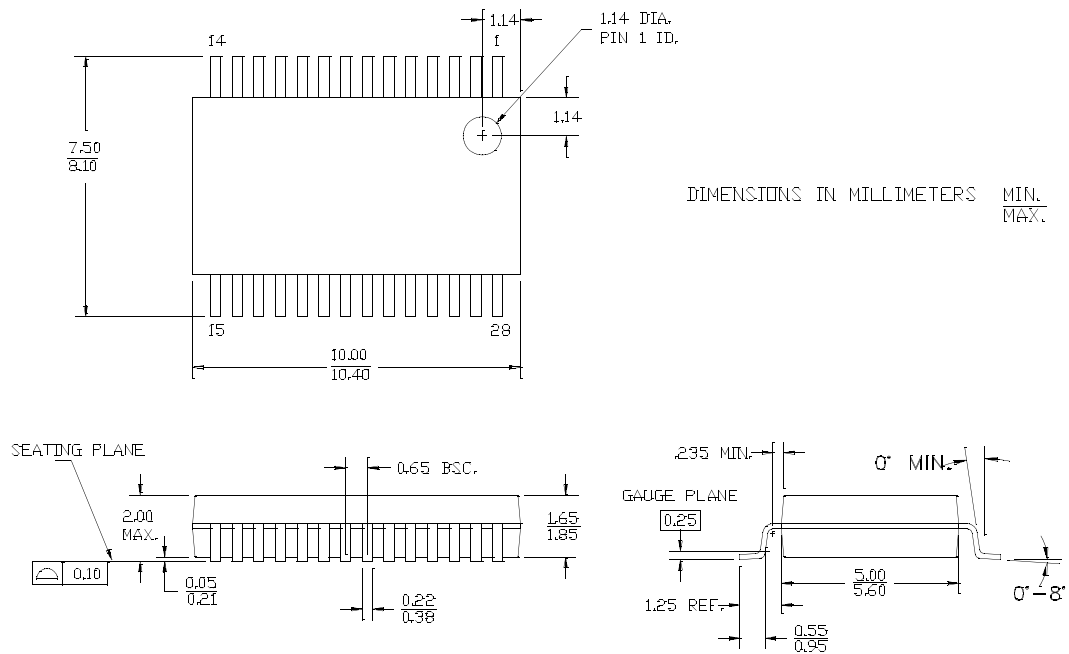
**NOTES:**

1.  HATCH AREA IS SOLDERABLE EXPOSED PAD
2. BASED ON REF JEDEC # MO-248
3. PACKAGE WEIGHT: 0.0388g
4. DIMENSIONS ARE IN MILLIMETERS [MIN/MAX]
5. MAXIMUM ALLOWABLE BURRS IS 0.076mm IN ALL DIRECTIONS.
6. PACKAGE CODE

PART NO.	DESCRIPTION
LR32D	STANDARD
LQ32D	PB-FREE

001-42168 \*A

Figure 20. 28-Pin (210-Mil) SSOP



51-85079 °C

### Thermal Impedances

Table 36. Thermal Impedances by Package

Package	Typical $\theta_{JA}$ [22]
32 QFN	19.4 °C/W
28 SSOP	95 °C/W

### Capacitance on Crystal Pins

Table 37. Typical Package Capacitance on Crystal Pins

Package	Package Capacitance
32 QFN	2.0 pF
28 SSOP	2.8 pF

### Solder Reflow Peak Temperature

Following is the minimum solder reflow peak temperature to achieve good solderability.

Table 38. Solder Reflow Peak Temperature

Package	Minimum Peak Temperature [23]	Maximum Peak Temperature
32 QFN	240°C	260°C
28 SSOP	240°C	260°C

#### Notes

22.  $T_J = T_A + \text{POWER} \times \theta_{JA}$ .

23. Higher temperatures may be required based on the solder melting point. Typical temperatures for solder are  $220 \pm 5^\circ\text{C}$  with Sn-Pb or  $245 \pm 5^\circ\text{C}$  with Sn-Ag-Cu paste. Refer to the solder manufacturer specifications.

## Ordering Information

The following table lists the CY8C23X33 PSoC device family key package features and ordering codes.

**Table 39. CY8C23X33 PSoC Device Family Key Features and Ordering Information**

Package	Ordering Code	Flash (Kbytes)	RAM (Bytes)	Temperature Range	Digital Blocks (Rows of 4)	Analog Blocks (Columns of 3)	Digital IO Pins	Analog Inputs	Analog Outputs	XRES Pin
32 Pin QFN	CY8C23533-24LQXI	8	256	-40°C to +85°C	4	4	26	12	2	Yes
32 Pin QFN (Tape and Reel)	CY8C23533-24LQXIT	8	256	-40°C to +85°C	4	4	26	12	2	Yes
28 Pin (210 Mil) SSOP	CY8C23433-24PVXI	8	256	-40°C to +85°C	4	4	26	12	2	No
28 Pin (210 Mil) SSOP (Tape and Reel)	CY8C23433-24PVXIT	8	256	-40°C to +85°C	4	4	26	12	2	No

## Document History Page

Document Title: CY8C23433, CY8C23533 PSoC® Mixed-Signal Array Document Number: 001-44369				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	2044848	KIY		Datasheet creation
*A	2482967	HMI/AESA	05/14/2008	Moved from Preliminary to Final. Part number changed to CY8C23433, CY8C23533. Adjusted placement of the block diagram; updated description of DAC; updated package pinout description, updated POR and LVD spec, Added Csc , Flash Vdd, SAR ADC spec. Updated package diagram 001-42168 to *A. Updated data sheet template.

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